Fundamentals of Digital System Testing

LIRMM

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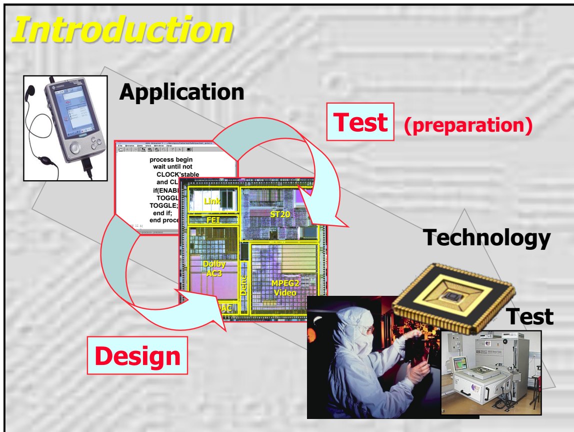
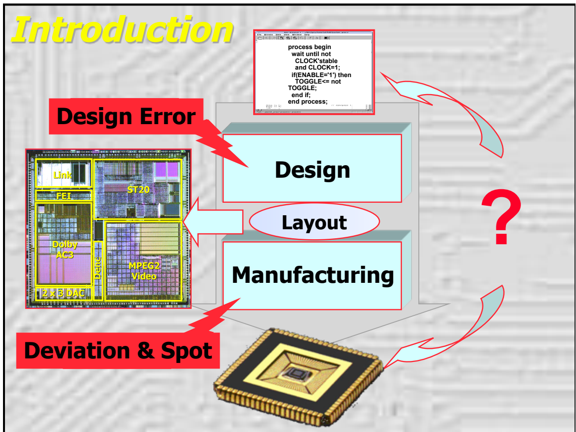
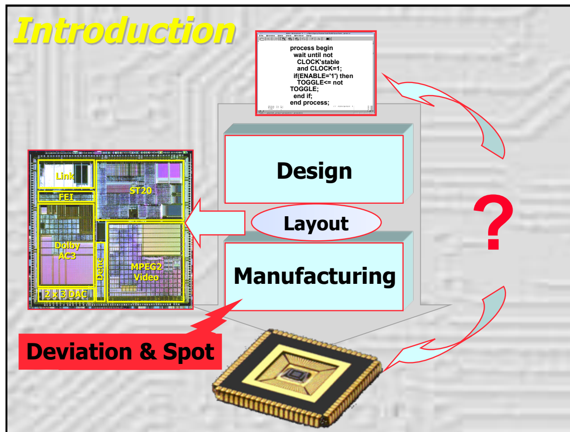
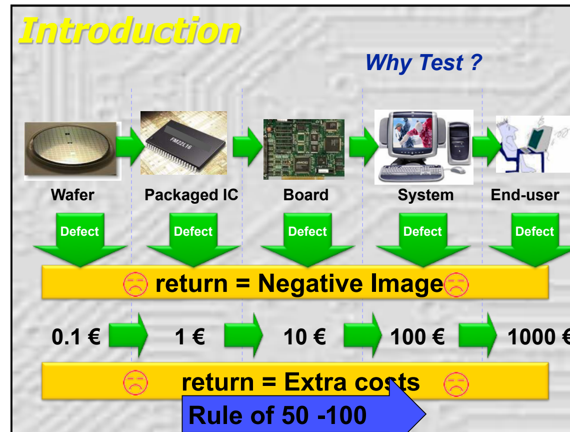
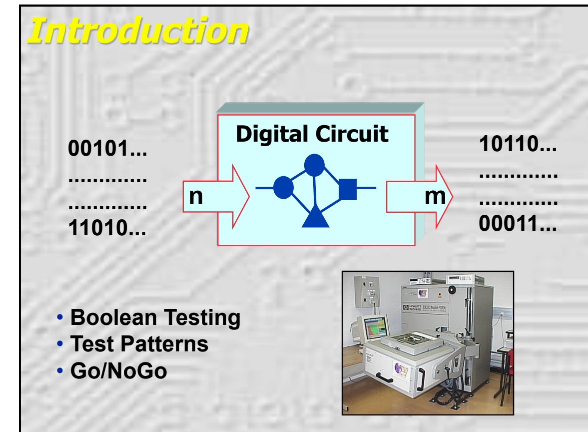
ARCHI'13





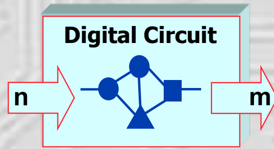

Introduction
Design
Layout
Manufacturing
?
Deviation & Spot


Introduction
Why Test ?
Wafer
Packaged IC
Board
System
End-user
Defect
Defect
Defect
Defect
Defect
return = Negative Image
0.1 €
1 €
10 €
100 €
1000 €
return = Extra costs
Rule of 50 -100


Introduction
00101...
....
....
11010...
n
Digital Circuit
m
10110...
....
....
00011...
• Boolean Testing
• Test Patterns
• Go/NoGo

Introduction

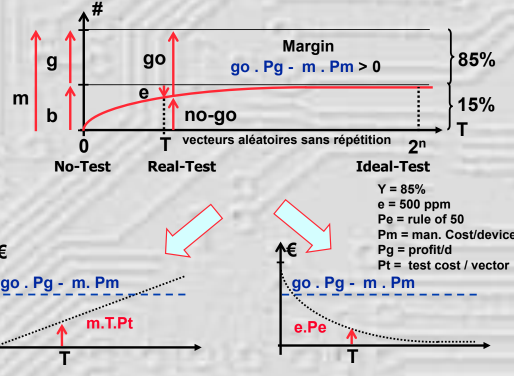
00101...
....
....
11010...



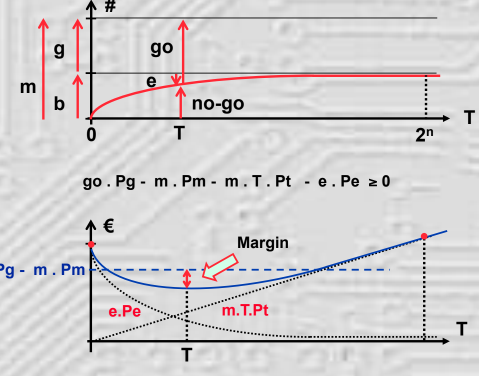
10110...
....
....
00011...

- Exhaustive Testing
- 2^{64} patterns
- 10^{20}/100MHz = 10^{12}s
- => 5850 years

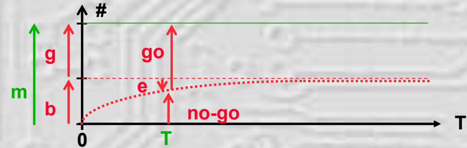
Introduction



Introduction

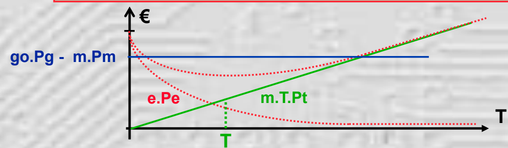


Introduction

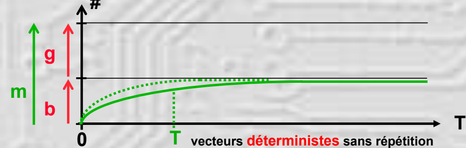


1 Criteria to stop the test generation

=> Estimate how many faulty circuits not yet detected (e?)

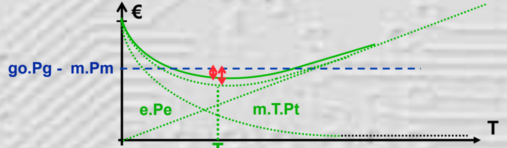


Introduction

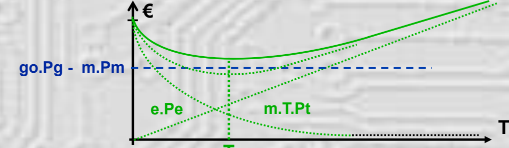


2 Criteria to optimize the test generation

=> Estimate how many faulty circuits are detected by each vector

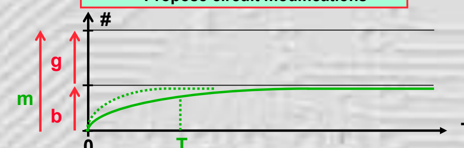


Introduction



3 Criteria to make circuit Testable

=> Propose circuit modifications

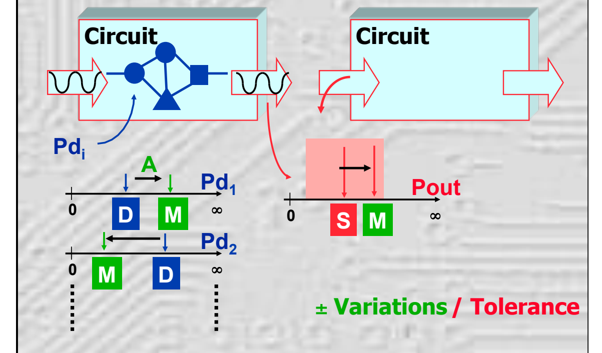


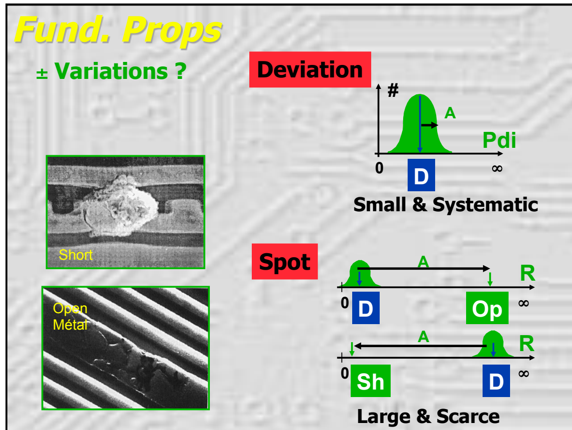
Introduction - Challenges

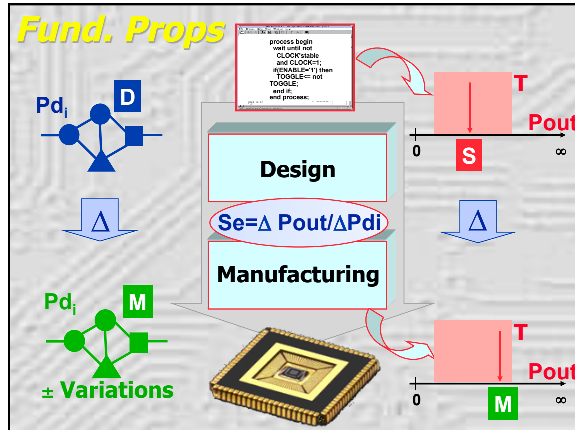
1. Criteria to stop the test generation
   => Estimate how many faulty circuits not yet detected (e?)
2. Criteria to optimize the test generation
   => Estimate how many faulty circuits are detected by each vector
3. Criteria to make circuit Testable
   => Propose circuit modifications

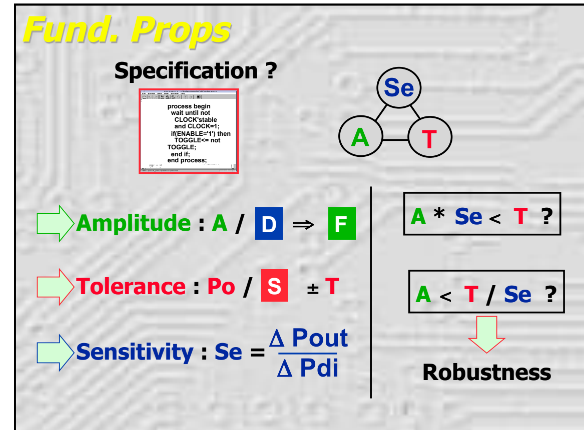
Fundamental Properties

Fund. Props




Fund. Props
± Variations ?
Deviation
#
A
Pdi
0
D
∞
Small & Systematic
Short
Open
Métal
Spot
A
R
0
D
Op
∞
A
R
0
Sh
D
∞
Large & Scarce


Fund. Props
Pdi
D
Δ
Pdi
M
± Variations
Design
Se=Δ Pout/ΔPdi
Manufacturing
T
Pout
0
S
∞
Δ
T
Pout
0
M
∞


Fund. Props
Specification ?
Se
A
T
Amplitude : A / D ⇒ F
Tolerance : Po / S ± T
Sensitivity : Se = Δ Pout / Δ Pdi
A * Se < T ?
A < T / Se ?
Robustness

Fund. Props

```
process begin
 wait until not
  CLOCK'stable
  and CLOCK=1;
 if(ENABLE='1') then
  TOGGLE<= not
 TOGGLE;
 end if;
end process;
```

Specification ?

A < T / Se ?

Robustness

Low T/Se	High T/Se
Deviations Small Systematic	
Spot Large Scarce	**Spot** Large Scarce

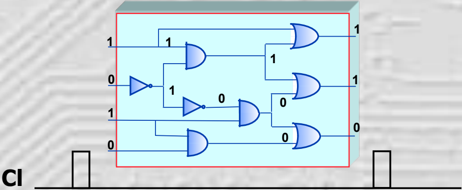
Fund. Props

Digital

```
process begin
 wait until not
  CLOCK'stable
  and CLOCK=1;
 if(ENABLE='1') then
  TOGGLE<= not
 TOGGLE;
 end if;
end process;
```

Specification ?

- Logic
- Timing



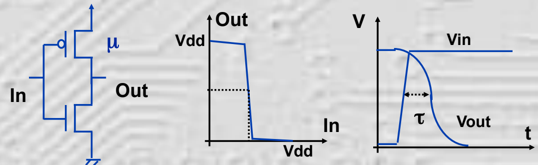
Fund. Props

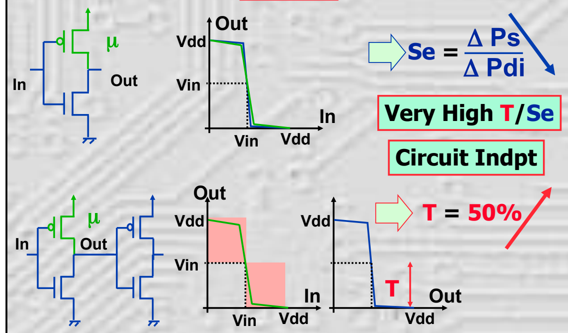
Digital

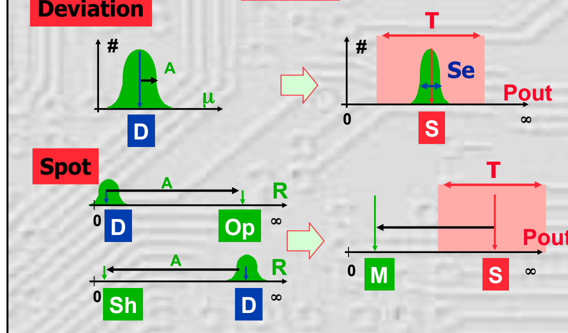
```
process begin
 wait until not
  CLOCK'stable
  and CLOCK=1;
 if(ENABLE='1') then
  TOGGLE<= not
 TOGGLE;
 end if;
end process;
```

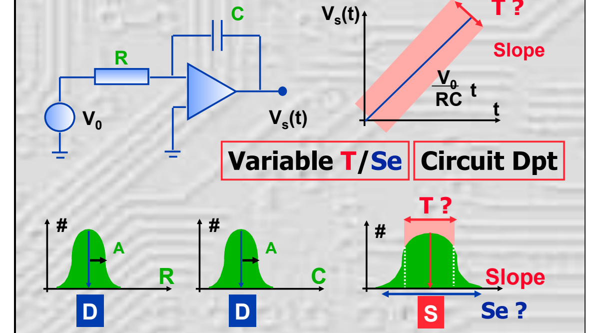
Specification ?

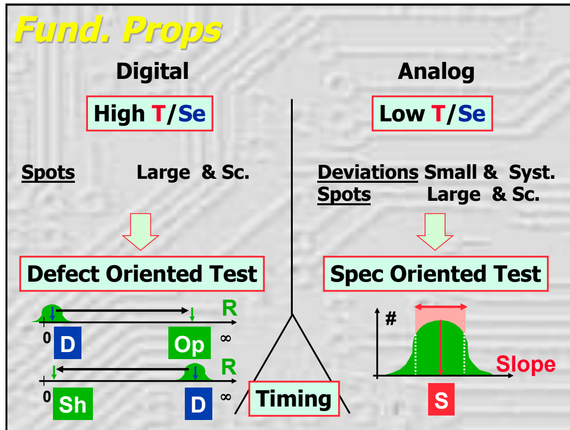
- Logic
- Timing

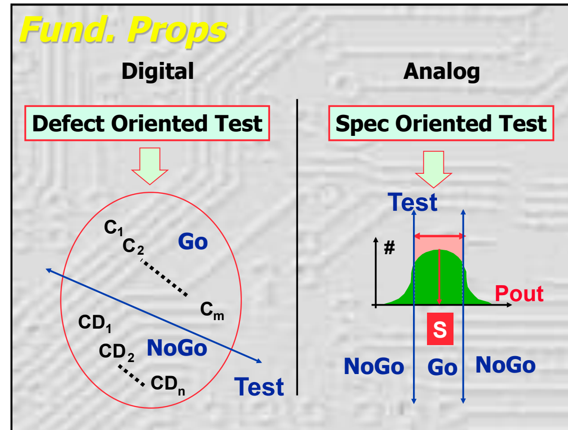


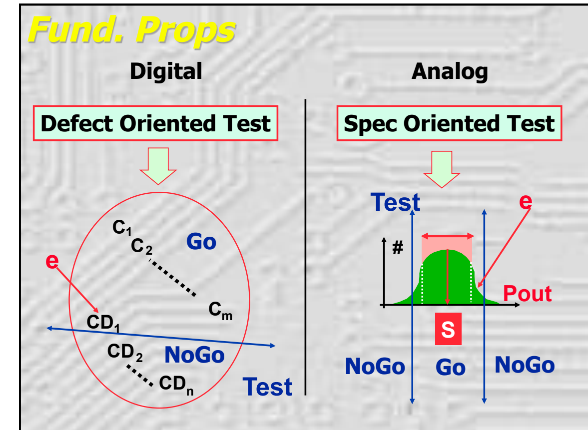

Fund. Props
Digital
In
μ
Out
Vdd
Out
Vin
In
Vin
Vdd
Se = Δ Ps / Δ Pdi
Very High T/Se
Circuit Indpt
In
μ
Out
Out
Vdd
Vin
In
Vin
Vdd
Vdd
T = 50%
T
Out
Vdd


Fund. Props
Digital
Deviation
#
A
μ
D
#
T
Se
Pout
0
S
∞
Spot
A
R
0
D
Op
∞
T
Pout
A
R
0
Sh
D
∞
0
M
S
∞

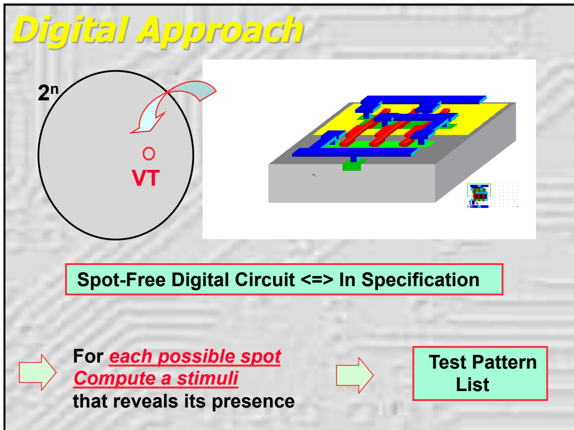

Fund. Props
Analog
C
R
V0
Vs(t)
Vs(t)
T ?
Slope
V0/RC t
t
Variable T/Se
Circuit Dpt
#
A
R
D
#
A
C
D
T ?
#
Slope
S
Se ?

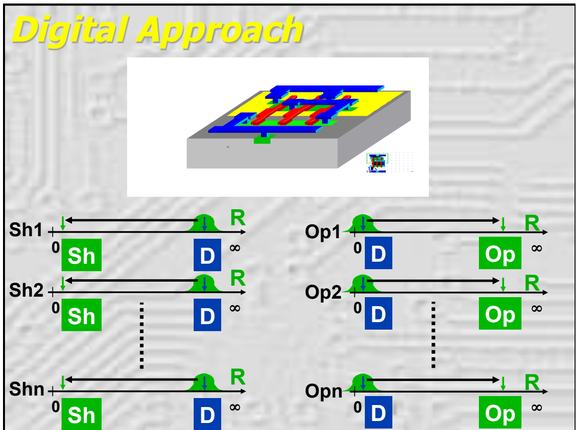

Fund. Props
Digital
Analog
High T/Se
Low T/Se
Spots
Large & Sc.
Deviations Small & Syst.
Spots Large & Sc.
Defect Oriented Test
Spec Oriented Test
R
0
D
Op
∞
R
0
Sh
D
∞
Timing
#
Slope
S


Fund. Props
Digital
Analog
Defect Oriented Test
Spec Oriented Test
C1
C2
Go
Cm
CD1
CD2
NoGo
CDn
Test
#
Pout
S
NoGo
Go
NoGo

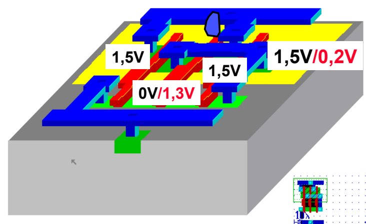

Fund. Props
Digital
Analog
Defect Oriented Test
Spec Oriented Test
e
C1
C2
Go
Cm
CD1
CD2
NoGo
CDn
Test
e
#
Pout
S
NoGo
Go
NoGo

Digital Approach

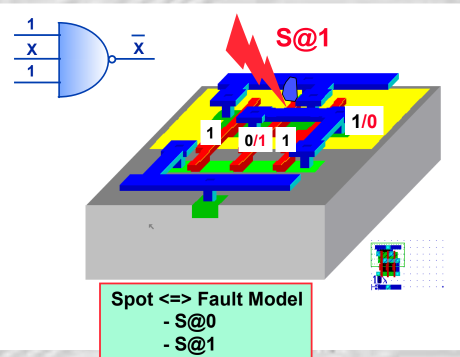




Digital Approach

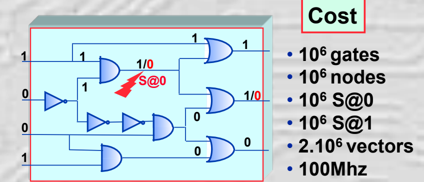


Digital Approach



Spot <=> Fault Model
- S@0
- S@1

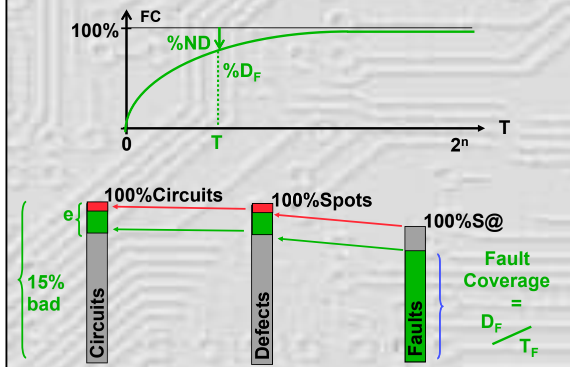
Digital Approach

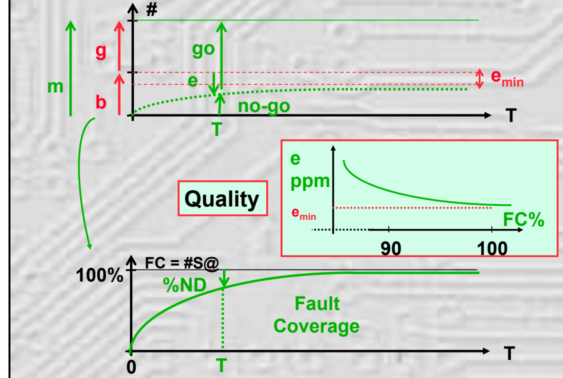


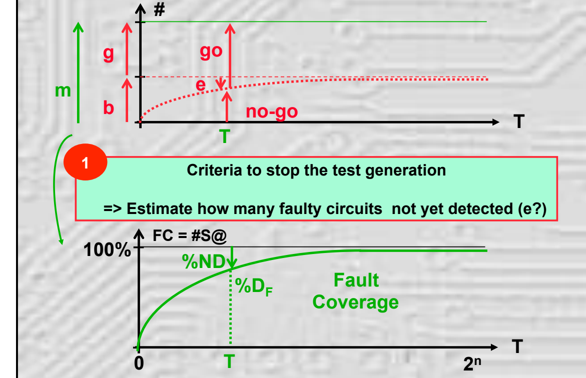
Cost

- 10^6 gates
- 10^6 nodes
- 10^6 S@0
- 10^6 S@1
- 2.10^6 vectors
- 100Mhz

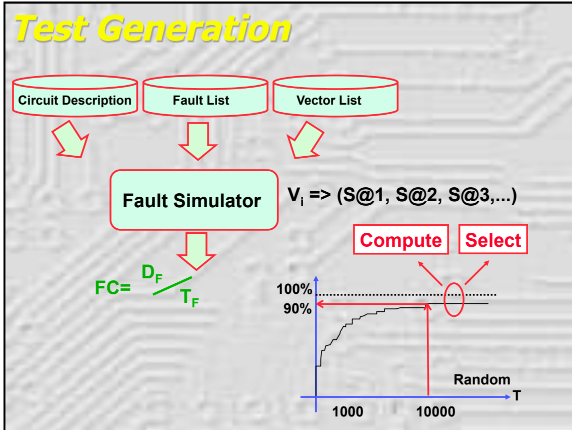
Physical Structure <=> Logical Structure
- Each Logic node S@0
- Each Logic node S@1
- TPG

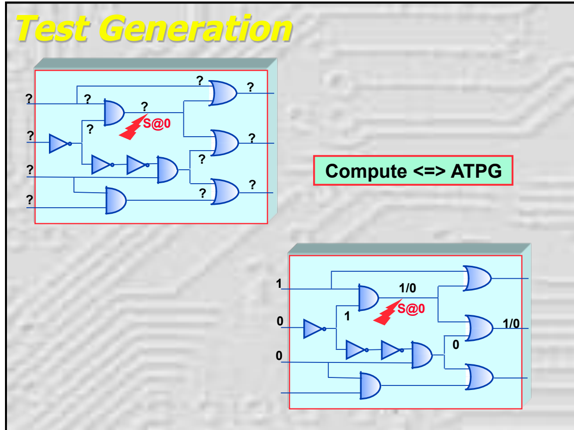

Digital Approach
FC
100%
%ND
%D_F
0
T
2^n
T
100%Circuits
100%Spots
100%S@
e
15%
bad
Circuits
Defects
Faults
Fault
Coverage
=
D_F
T_F


Digital Approach
#
m
g
b
go
e
no-go
e_{min}
T
T
Quality
e
ppm
e_{min}
FC%
90
100
100%
FC = #S@
%ND
Fault
Coverage
0
T
T

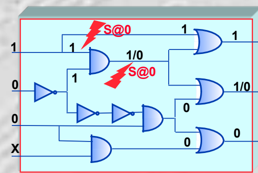

Digital Approach
#
m
g
b
go
e
no-go
T
T
1
Criteria to stop the test generation
=> Estimate how many faulty circuits not yet detected (e?)
100%
FC = #S@
%ND
%D_F
Fault
Coverage
0
T
2^n
T

Test Generation





Test Generation



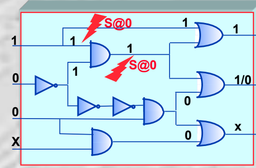
T_9

S_8 S_{82} S_{45} S_{112} S_{57} S_{80}

S_{13}

T_3 T_{28} T_{44} T_{11} T_{70} T_{829}

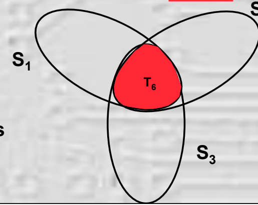
Test Generation



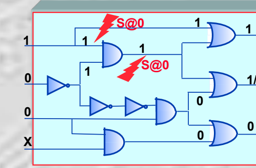
Cost

- Desired e (Application)
- Desired FC%
- Structural ATPG => Vectors
- Minimal number

S_1 S_2 S_3



Test Generation



FC 90%

- S@1 => S1=(T_{11} or T_{12} or T_{13} ...)
- S@2 => S2=(T_{21} or T_{22} or T_{23} ...)
- S@3 => S3=(T_{31} or T_{32} or T_{33} ...)
- ....

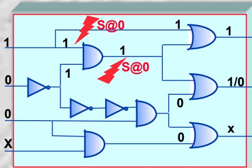
FC 98%

S1 and S2 and S3 and ..

$T=(T_1 + T_2 + T_3)(T_1)(T_2 + T_4)$

$T = T_1T_2 + T_1T_2T_3 + T_1T_4 + T_1T_2T_4 + T_1T_3T_4$

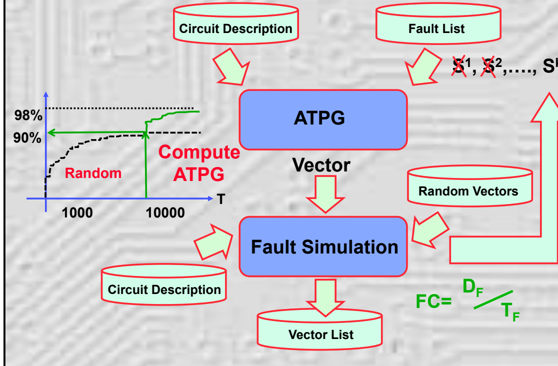
Test Generation



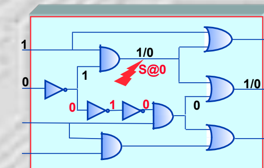
Cost

- ATPG :
  S@1 => T_{11} (np)
- Fault Simulation :
  V_{ij} => (S@1, S@2, S@3, S@4 ...) (ok)

Test Generation



Test Generation

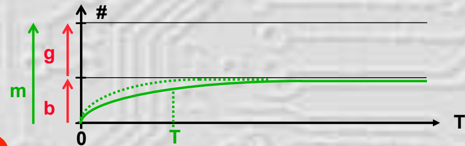


- Backward justification
- Conflict
- Backtrack

⇒

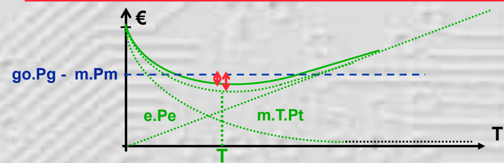
- Limited number Backtrack
- Fault abandon

Test Generation



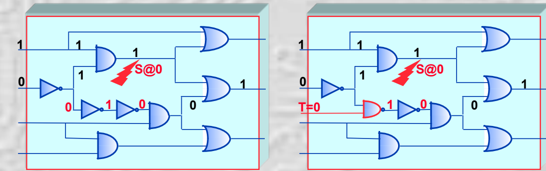
2 Criteria to optimize the test generation

=> Estimate how many faulty circuits are detected by each vector



Design For Testability

DFT

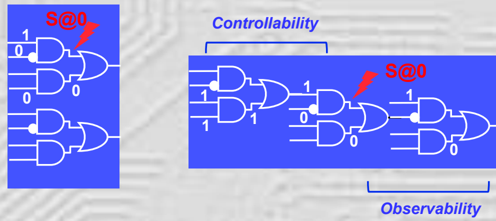


- ATPG / Backtrack
- FC < Desired FC (98%)
- Modify the Structure

Design For Test

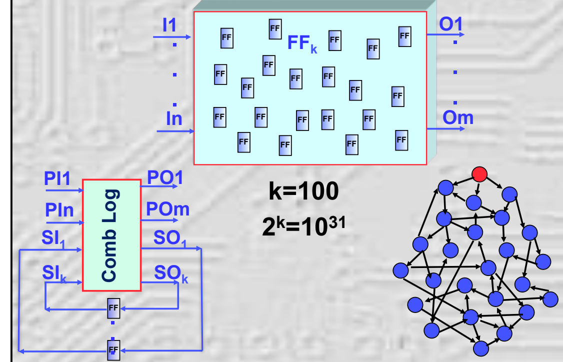
Structured DFT

Combinational Logic



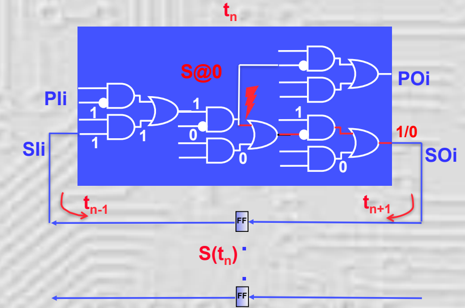
Structured DFT

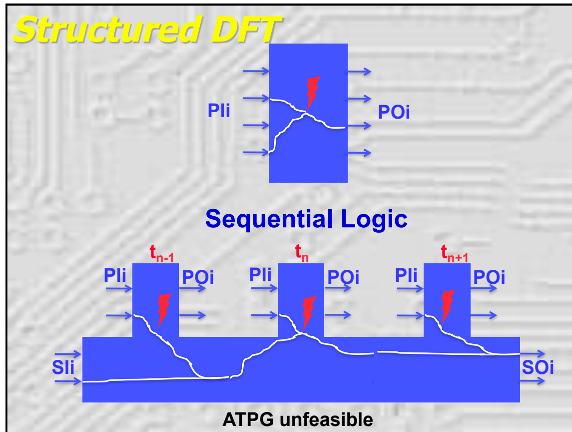
Sequential Logic

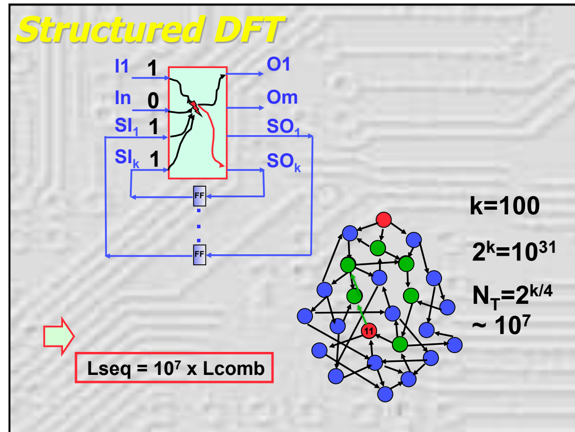


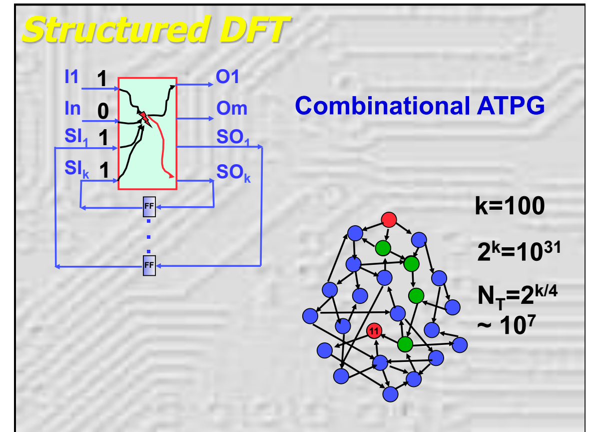
Structured DFT

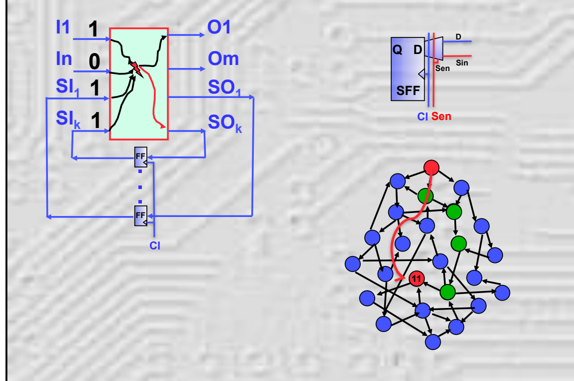
Sequential Logic

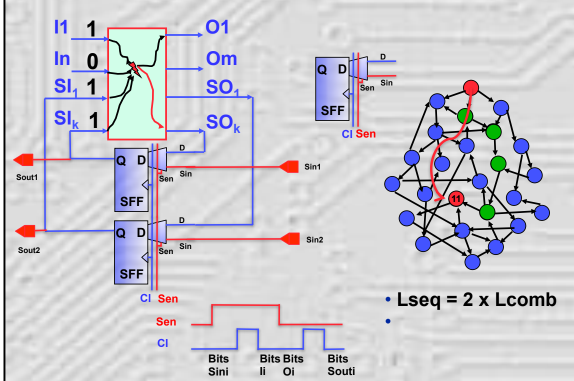


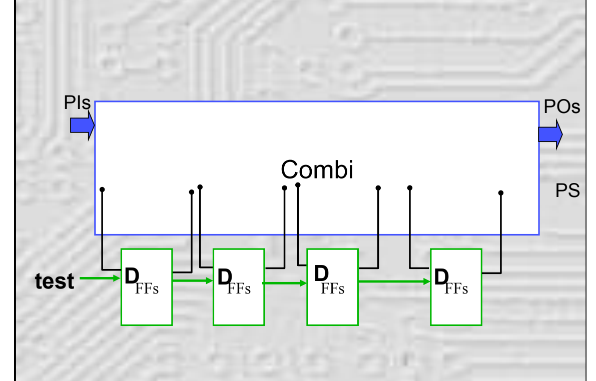

Structured DFT
PIi
POi
Sequential Logic
t_{n-1}
t_n
t_{n+1}
PIi
POi
PIi
POi
PIi
POi
SIi
SOi
ATPG unfeasible

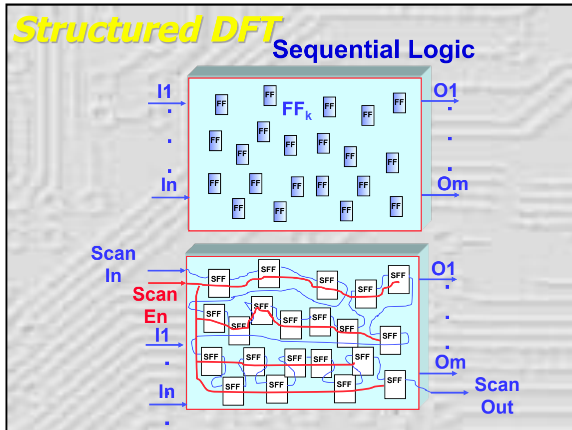

Structured DFT
I1 1
In 0
SI_1 1
SI_k 1
O1
Om
SO_1
SO_k
k=100
$2^k=10^{31}$
$N_T=2^{k/4}$
~ 10^7
Lseq = 10^7 x Lcomb

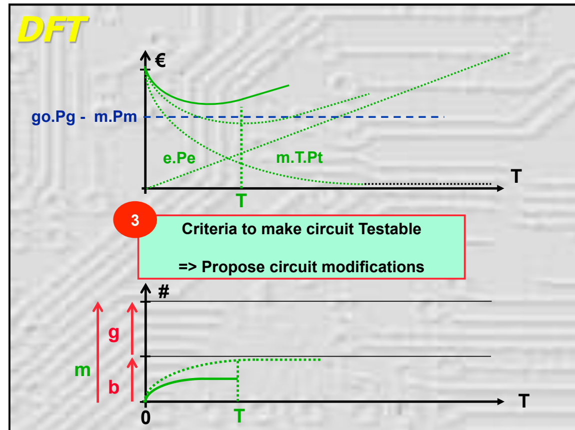

Structured DFT
I1 1
In 0
SI_1 1
SI_k 1
O1
Om
SO_1
SO_k
Combinational ATPG
k=100
$2^k=10^{31}$
$N_T=2^{k/4}$
~ 10^7

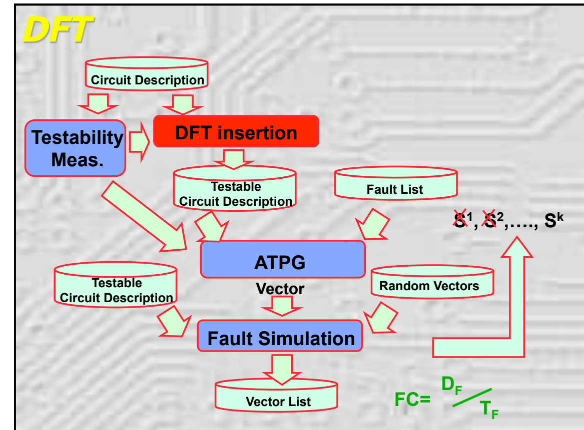

Structured DFT
I1 1
In 0
SI1 1
SIk 1
O1
Om
SO1
SOk
FF
FF
CI
Q D
SFF
Sen
Sin
D
CI Sen
I1

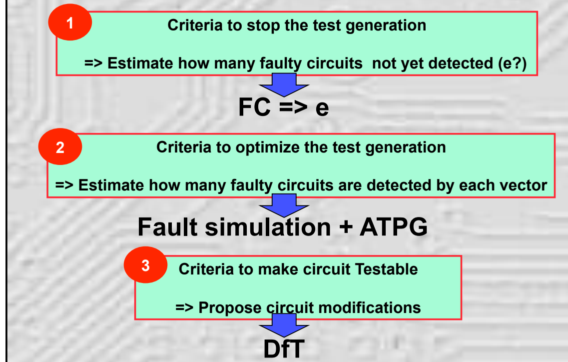

Structured DFT
I1 1
In 0
SI1 1
SIk 1
O1
Om
SO1
SOk
Sout1
Sout2
Q D
SFF
Sen
Sin
D
Sin1
Sin2
CI Sen
Sen
CI
Bits Sini
Bits Ii
Bits Oi
Bits Souti
Lseq = 2 x Lcomb
I1


Structured DFT
PIs
POs
Combi
PS
test
D FFs
D FFs
D FFs
D FFs


Structured DFT
Sequential Logic
I1
In
FFk
O1
Om
Scan
In
Scan
En
I1
In
O1
Om
Scan
Out


DFT
€
go.Pg - m.Pm
e.Pe
m.T.Pt
T
T
3
Criteria to make circuit Testable
=> Propose circuit modifications
#
g
m
b
0
T
T


DFT
Circuit Description
Testability
Meas.
DFT insertion
Testable
Circuit Description
Fault List
ATPG
Vector
Testable
Circuit Description
Random Vectors
Fault Simulation
Vector List
FC=


Conclusion
1
Criteria to stop the test generation
=> Estimate how many faulty circuits not yet detected (e?)
FC => e
2
Criteria to optimize the test generation
=> Estimate how many faulty circuits are detected by each vector
Fault simulation + ATPG
3
Criteria to make circuit Testable
=> Propose circuit modifications
DfT