leti
innovation for industry

Electronique ultra basse consommation solutions adiabatiques

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MINATEC on the scientific polygone

Power aspects are nanoelectronics drivers

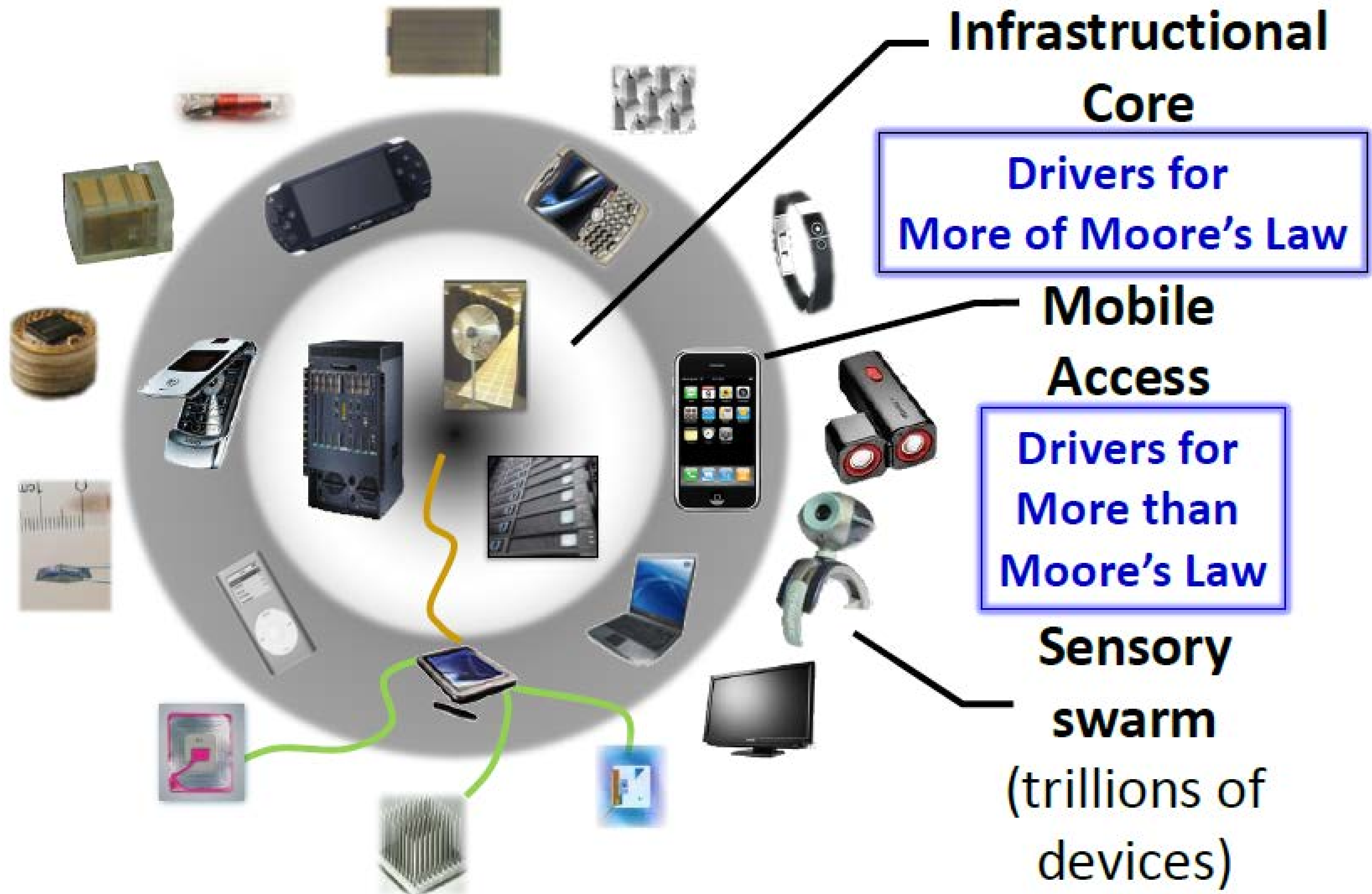
AMD motherboard with 1.1GHz 55 Watt Athlon Thunderbird

Courtesy of AMD

Why less power? TODAY

- access to powerful computation at any location
  - restrictions on size, weight and power
  - small, but powerful batteries
- increase in number of portables
  - notebook, laptop
  - games
  - mobile phones
  - mobile DVD players
  - MP3 players
  - GPS

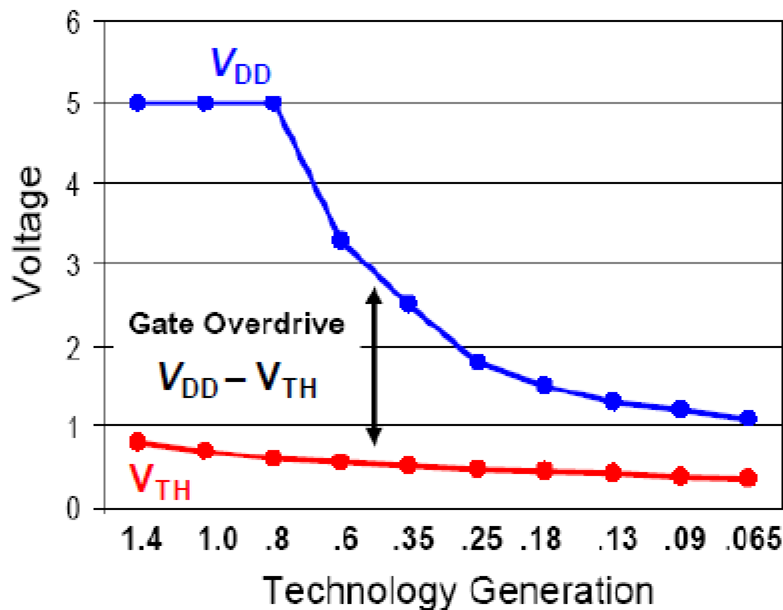
Why less power? TOMORROW



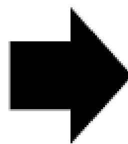
J. Rabaey, *ASPDAC* 2008

Unfortunately the power density is not decreasing with CMOS scaling

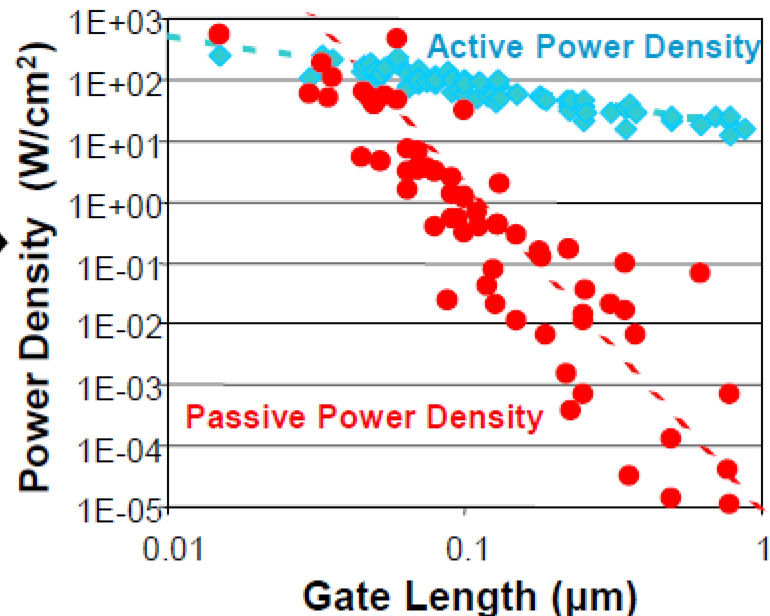
CMOS VOLTAGE SCALING



Source: P. Packan (Intel), 2007 IEDM Short Course



POWER DENSITY VS. GATE LENGTH



Source: B. Meyerson (IBM) Semico Conf., January 2004

- Power dissipation limitations are crucial for portable systems but also for supercomputers and all electronic applications
- How to solve this problem using nanocomponents ?
  - Decrease of capacitances and voltage…
  - Decrease of subthreshold current and tunnel effects…
  - New architectures….

OUTLINE

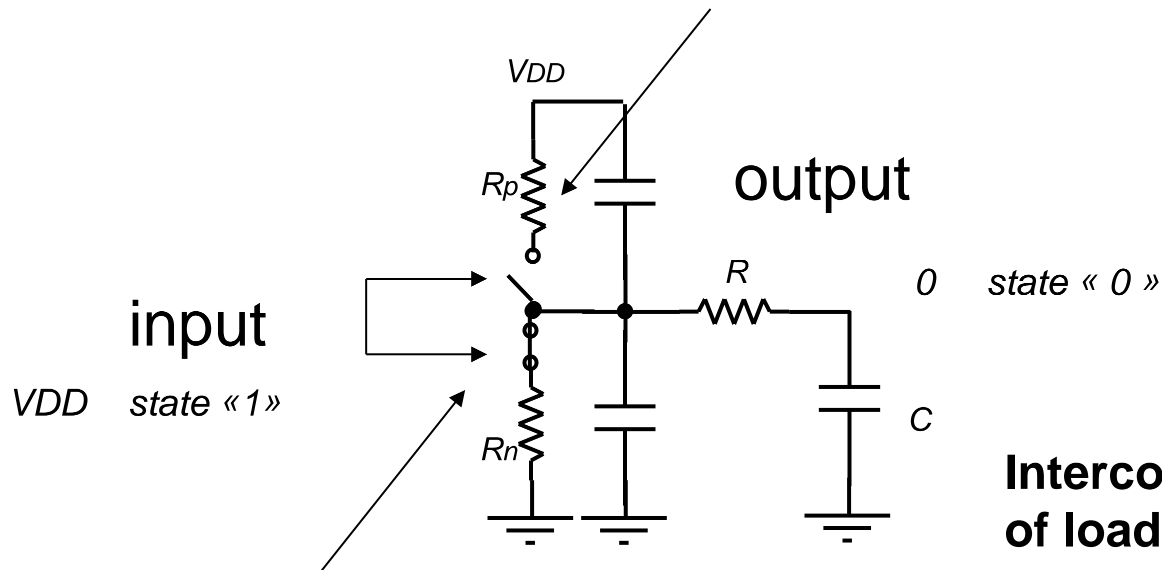
- CMOS: what is necessary to know…
- Power dissipation: static power and dynamic power
- Power optimization at component and circuit level
- Power dissipation at architecture level
- Adiabatic and reversible computing

- **CMOS: what is necessary to know…**
  - **PMOS and NMOS**
  - **Inverters and logical functions**
  - **The global architecture**
- Power dissipation: static power and dynamic power
- Power optimization at component and circuit level
- Power dissipation at architecture level
- Adiabatic and reversible computing

A basic function : the inverter

On if command is “0”

Off if command is “1”

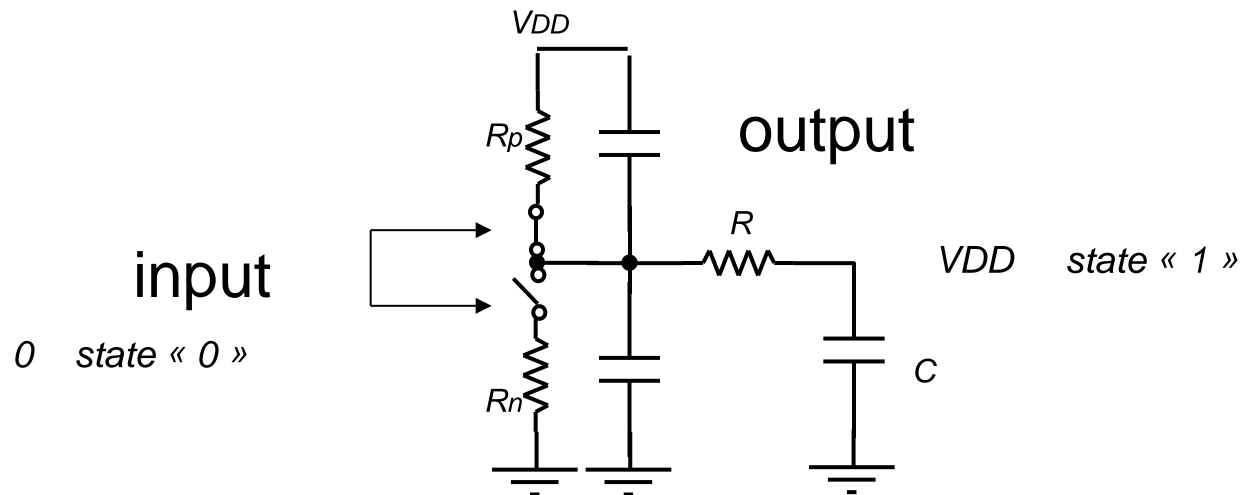


Interconnect and input of load gates

On if command is “1”

Off if command is “0”

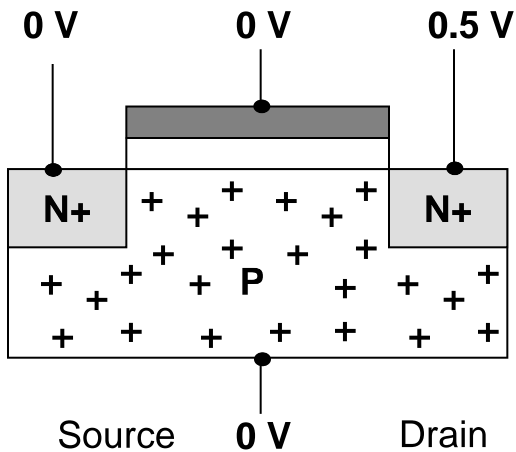
A basic function : the inverter



two different switches are necessary

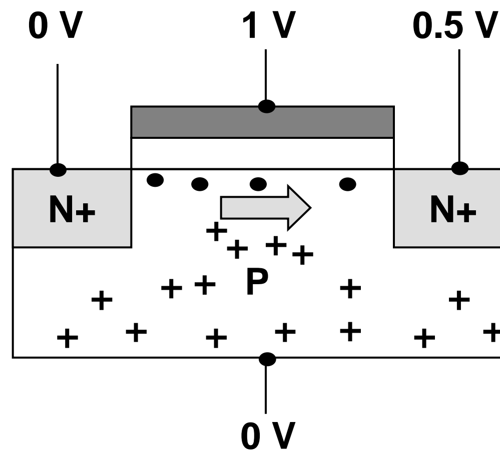
The NMOS transistor

under threshold



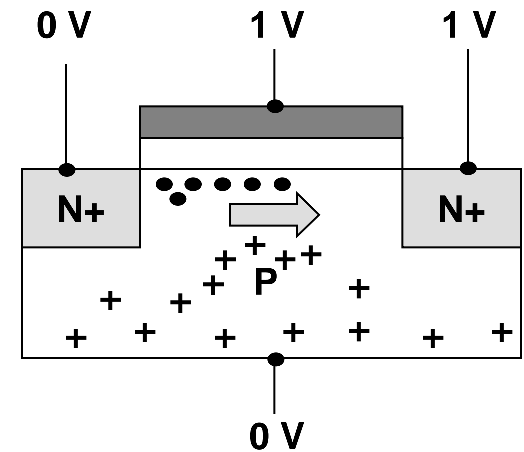
MOSFET OFF

above threshold



MOSFET ON

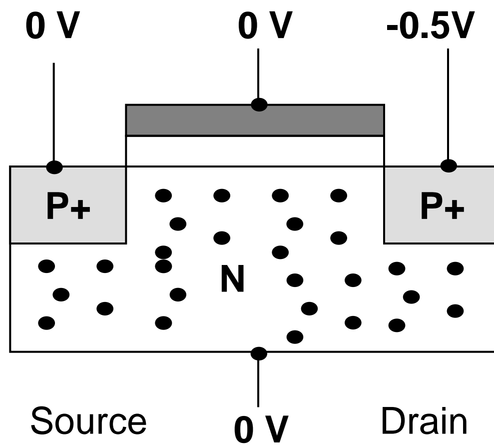
above threshold

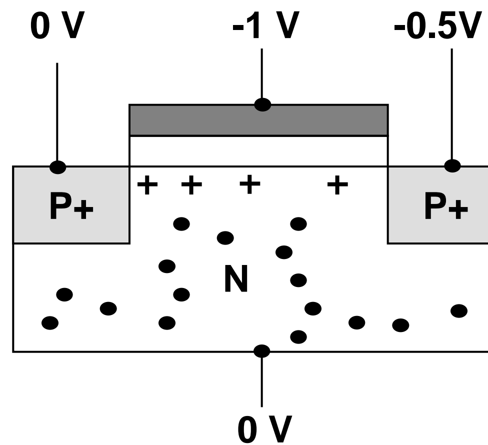


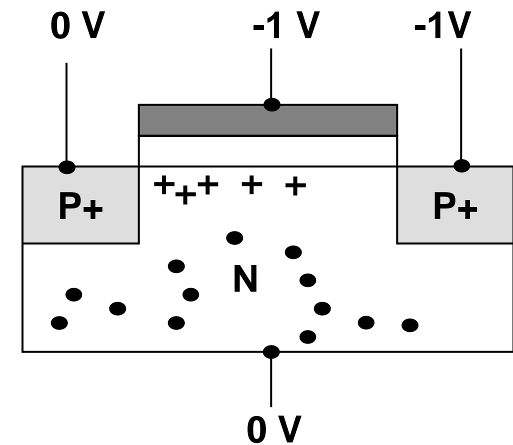
MOSFET ON and saturation

The PMOS transistor

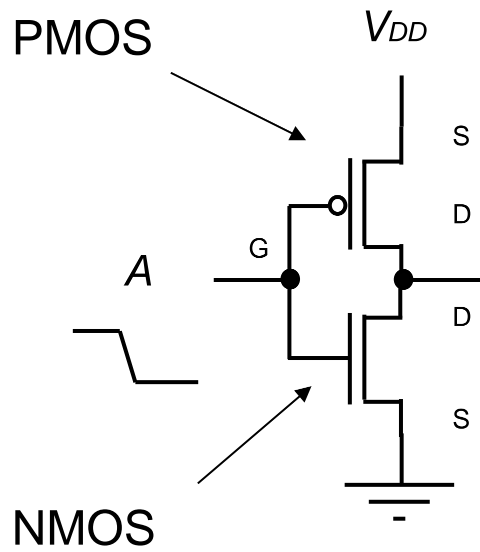
below threshold | above threshold | above threshold

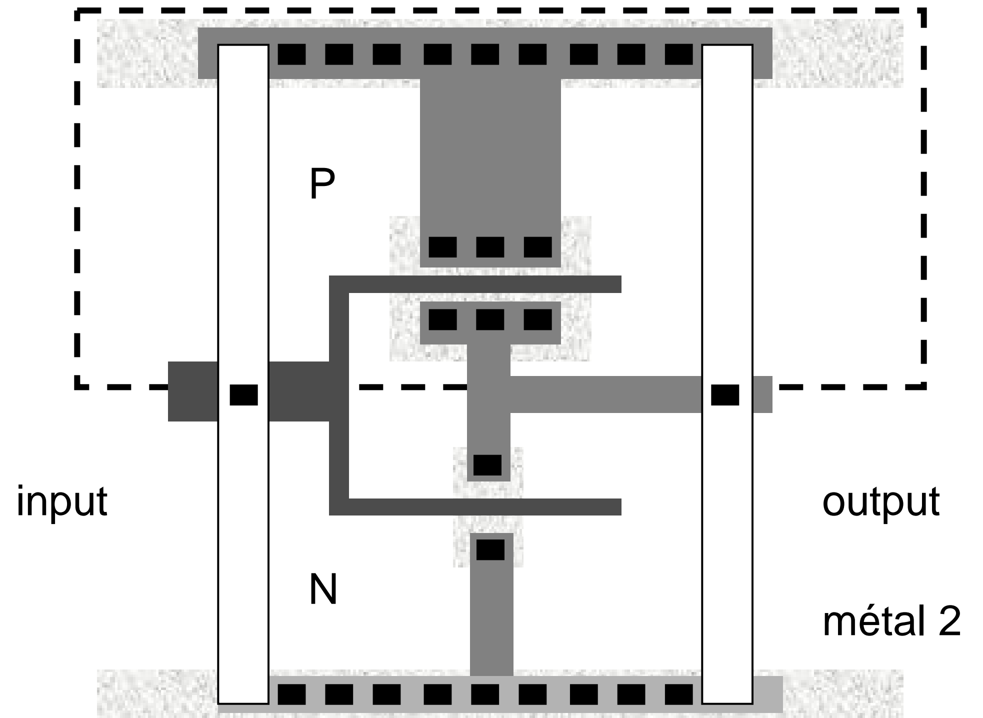


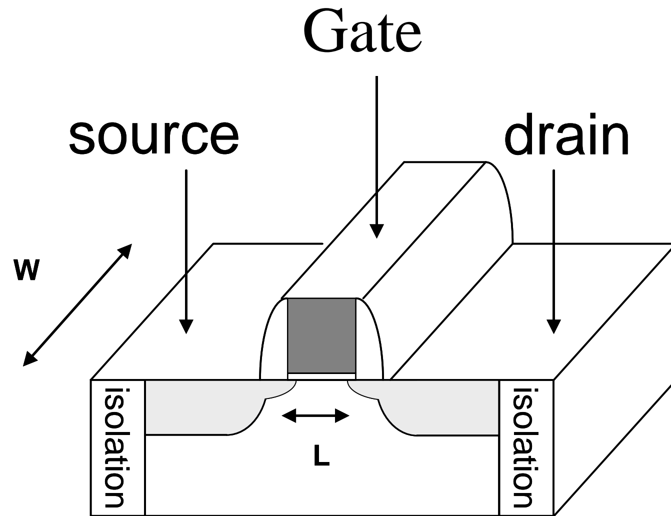




MOSFET OFF | **MOSFET ON** | **MOSFET ON and saturation**


PMOS
V_{DD}
S
D
G
A
D
S
NMOS


P
N
input
output
métal 2



L around 0,05 micron

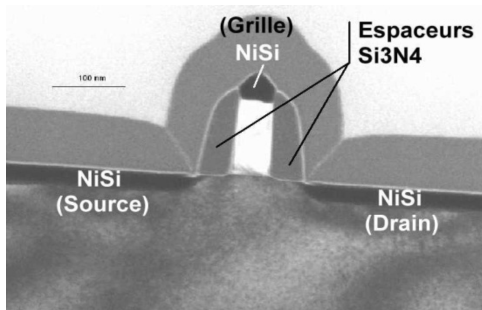
W between 0.05 and 0.5 micron (except for analog or buffering)

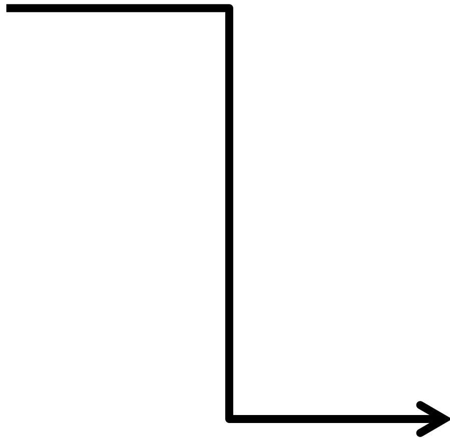
$$I_{on} = WC'_{OX} v_{sat} (V_{GS} - V_T)$$

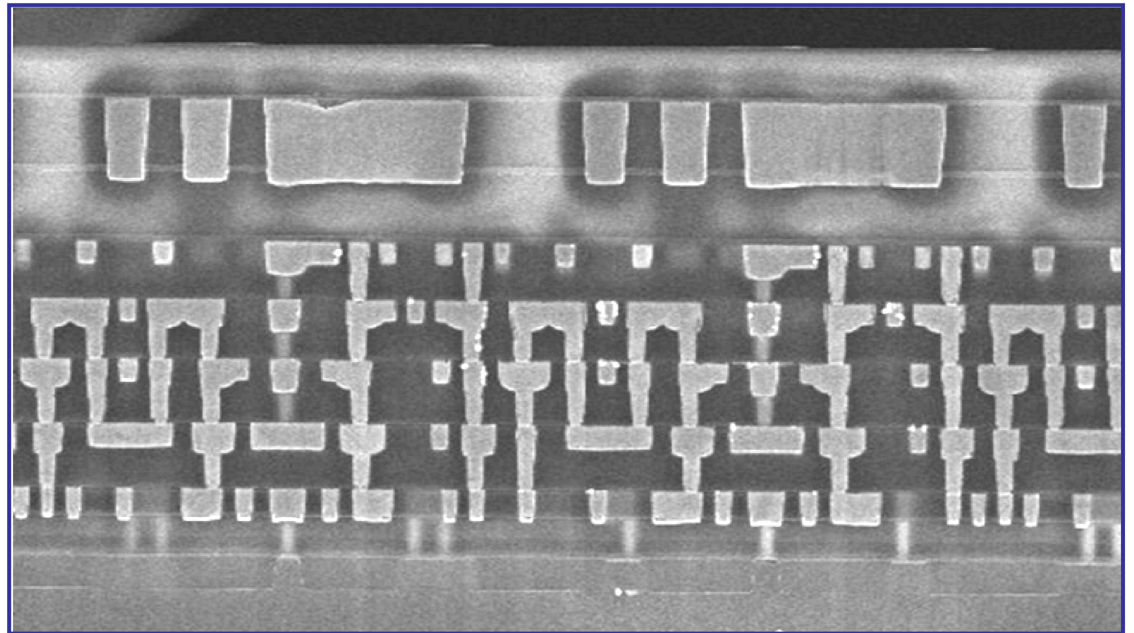
v_{sat} saturation velocity of carriers in the conduction channel

C'_{OX} capacitance per surface unit of the oxyde layer

V_T Threshold voltage

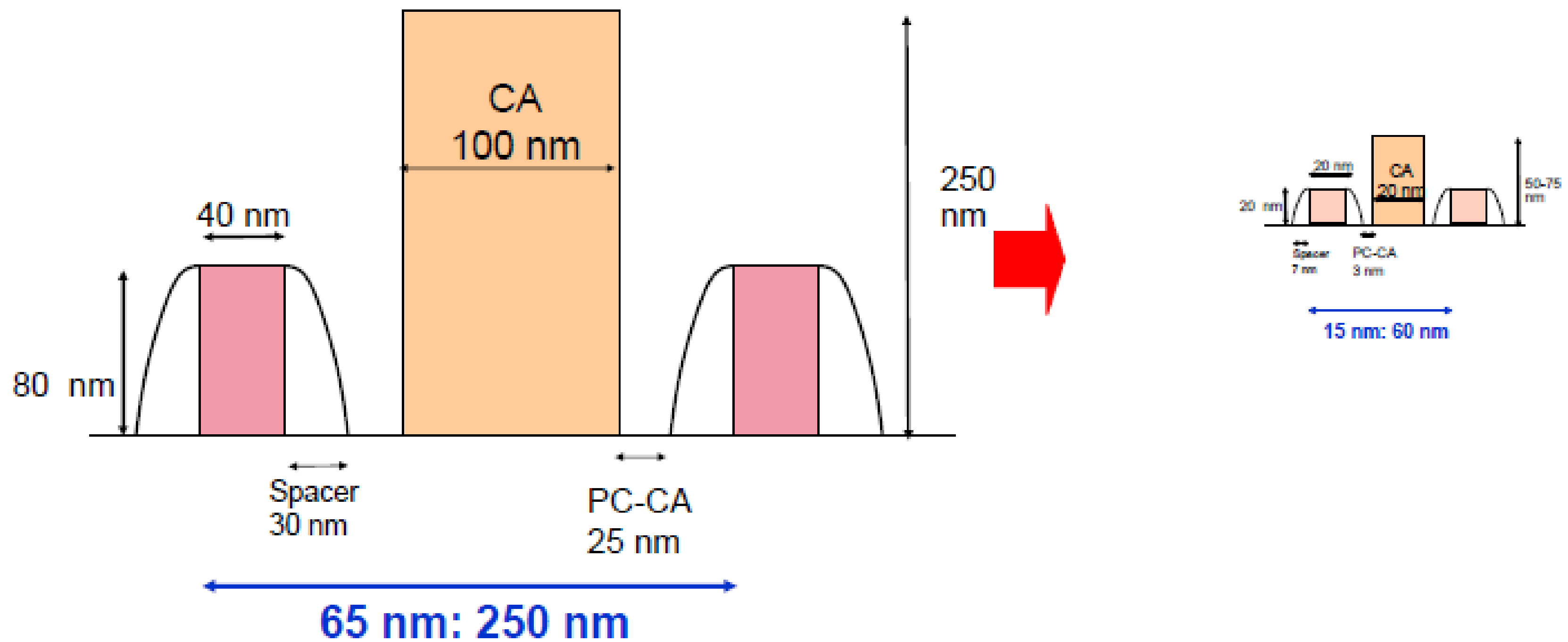




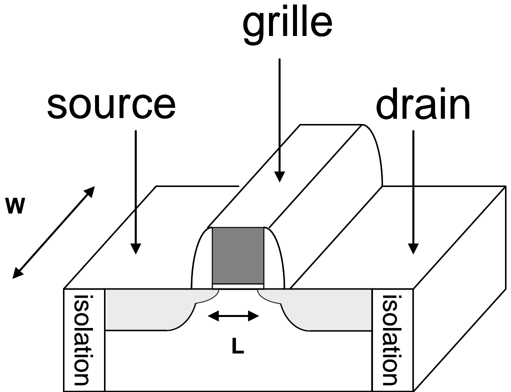


multilevel of metallization

The microelectronic scaling principle



The MOS transistor is a nanocomponent



Gate

1.2nm SiO_2

Silicon substrate

Gate

3.0nm High-k

Silicon substrate

Basic FET model

- The I_{on} current (short channel)

$$I_{on} = WC'_{OX} v_{sat} \left(V_{GS} - V_T\right)$$

- The I_{off} current

$$I_{off} = Wk \exp^{\frac{-V_T}{nV_{th}}} \left(1 - \exp^{-\frac{V_{DS}}{V_{th}}}\right)$$

Strong effect of threshold voltage

Tunnel current in addition

$$V_{th} = \frac{kT}{q}$$

The thermal voltage (25 mV at room temperature)

$$n = 1 + \frac{C_D}{C_n}$$

The body effect factor

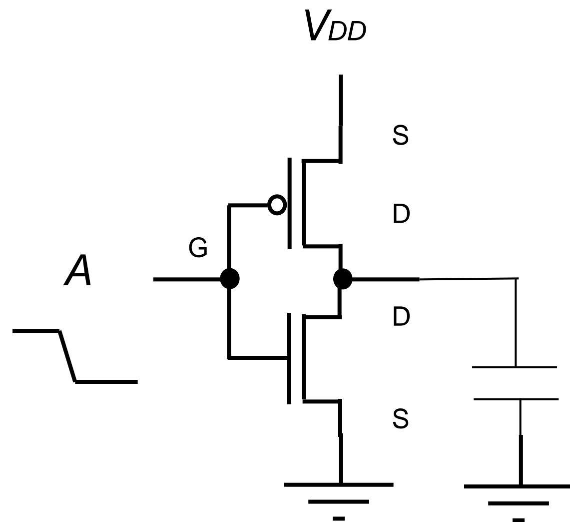
$C_n = WLC'_{OX}$

C_D depletion capacitance

Leti

Importance of *Ion* et *Ioff*

- ***Ioff*** **defines leakage power consumption**
- ***Ion*** **defines speed of the circuit**



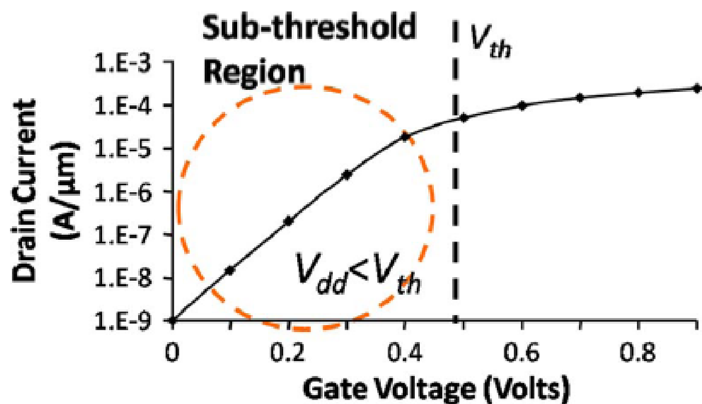
Charging time of the output capacitance

$$i = C\frac{\Delta V}{\Delta t}$$

Trade-off between speed and consumption

The different modes

- **Conventional and subthreshold modes**

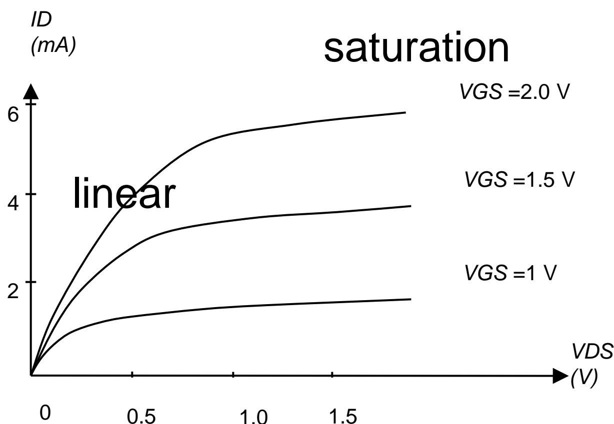


$$I_{sub} = n \cdot \mu \cdot \frac{C_n}{L^2} V_{th}{}^2 \exp^{\frac{V_{GS}-V_T}{nV_{th}}} \left(1 - \exp^{-\frac{V_{DS}}{V_{th}}}\right)$$

$$V_{th} = \frac{kT}{q}$$

$$n = 1 + \frac{C_D}{C_n} \quad C_n = WLC'_{OX} \quad C_D \text{ capacitance of the depeletion region}$$

- **Linear and saturation modes**



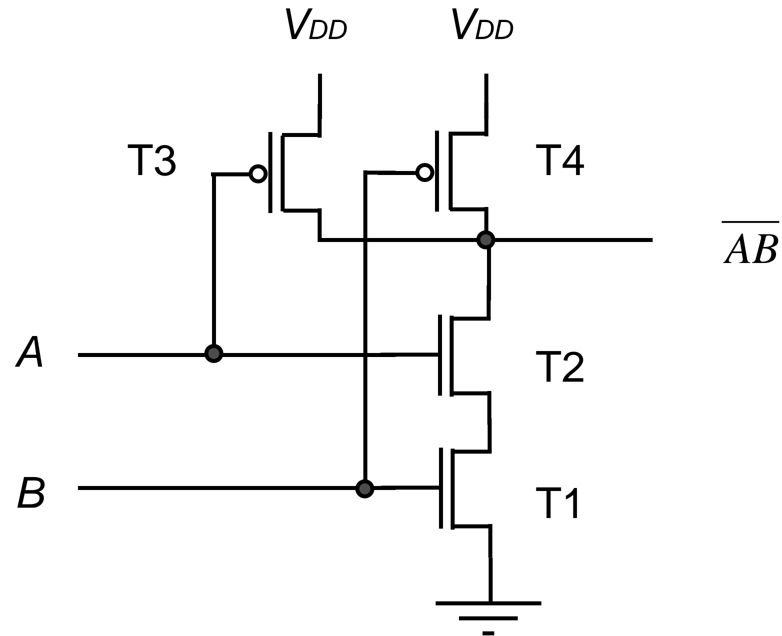
linear

$$I_{on} = \frac{W}{L} \mu \cdot C'_{OX} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}{}^2 \right]$$

saturation

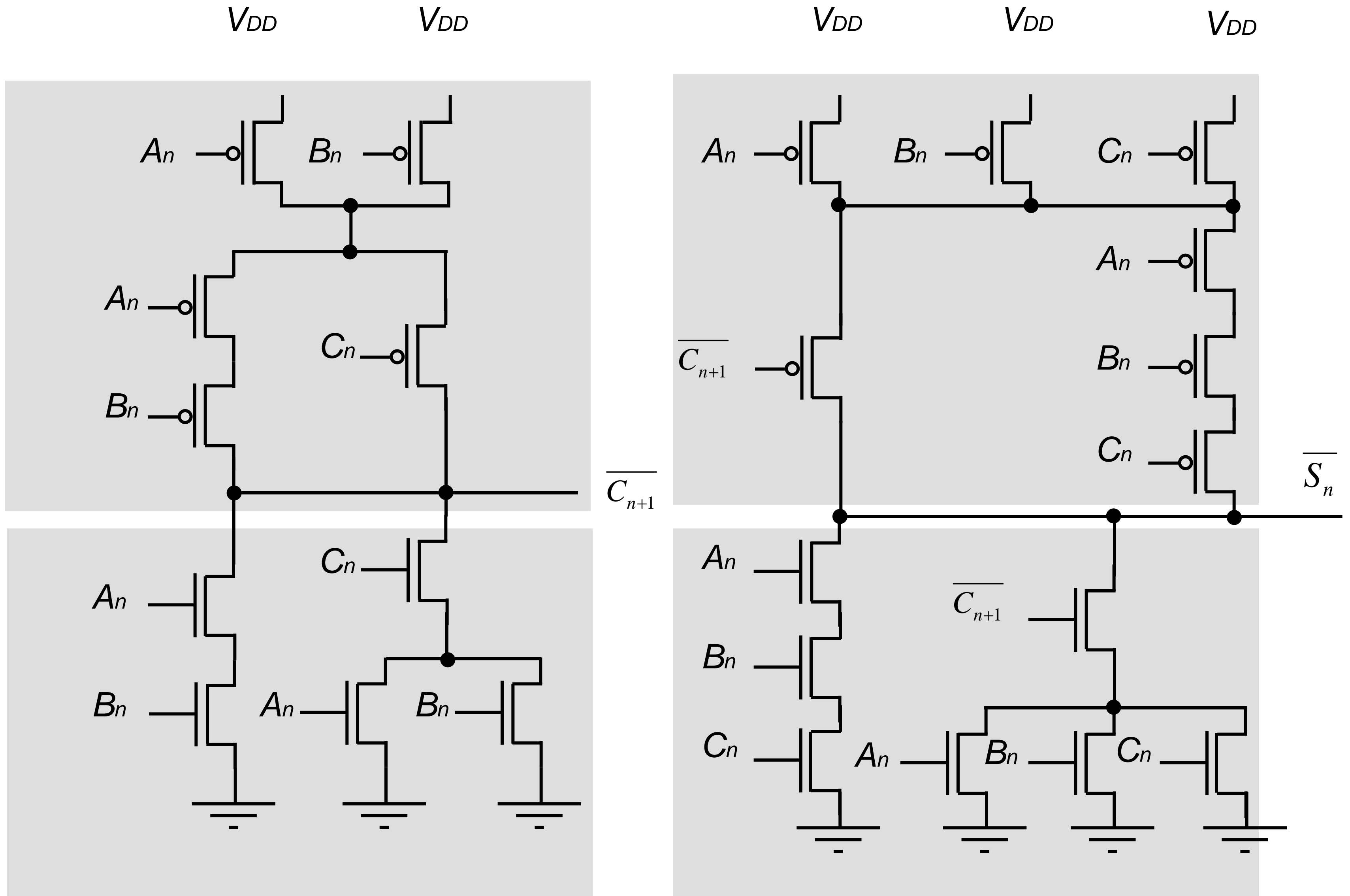
$$I_{on} = \frac{1}{2} \frac{W}{L} \mu \cdot C'_{OX} (V_{GS} - V_T)^2 \quad \text{or} \quad I_{on} = WC'_{OX} v_{sat} (V_{GS} - V_T - V_{DSsat})$$

An elementary function (NAND)

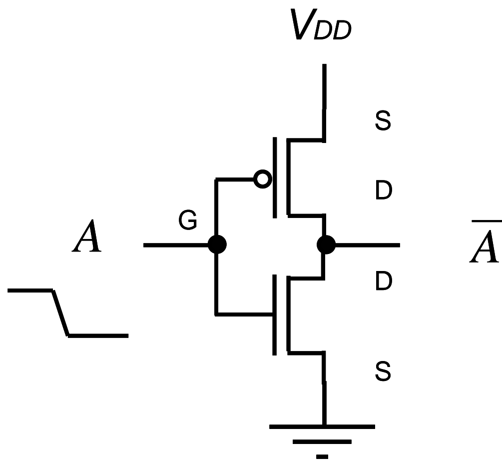


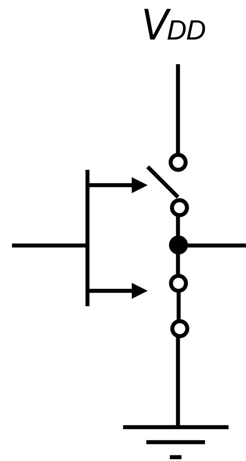
The inverter architecture

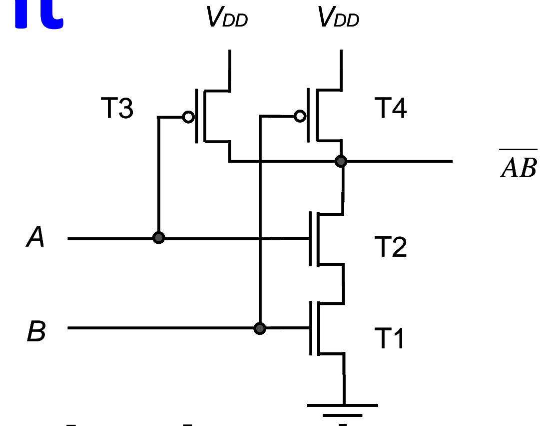
A more complex cell: the half adder



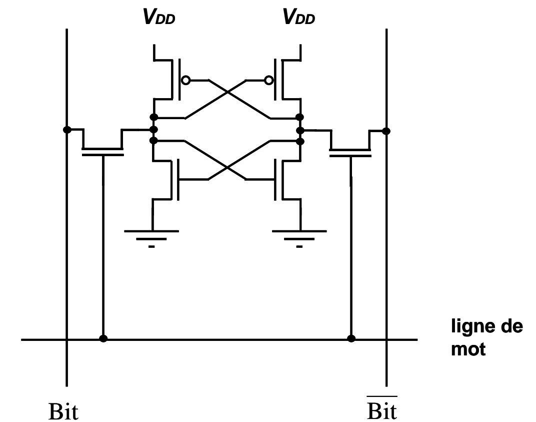
Now systems are switch based systems
Inverter is the basic element



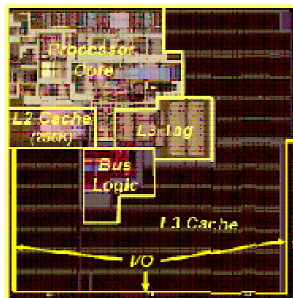


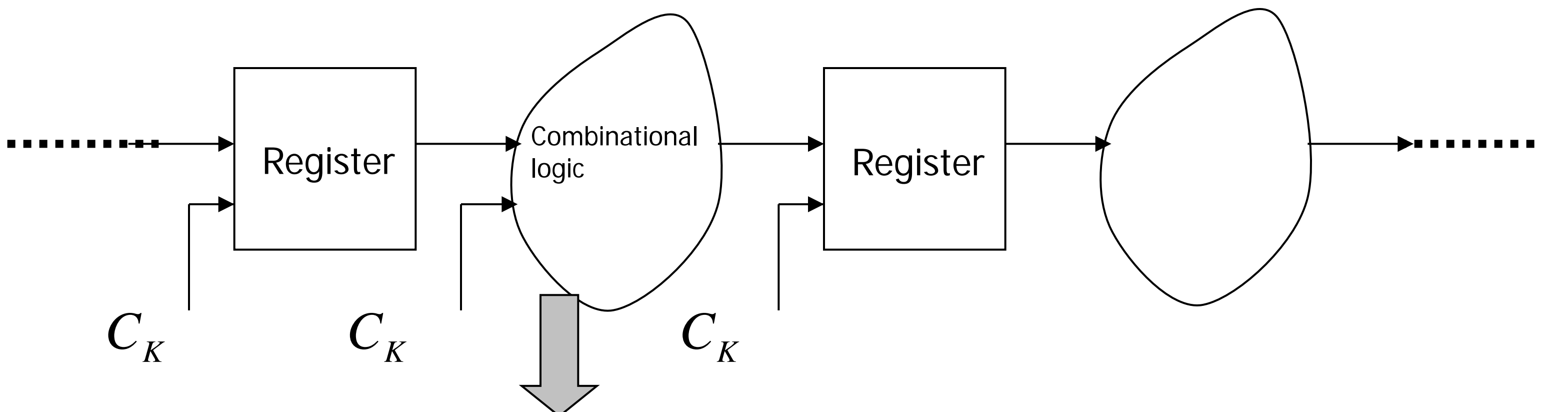


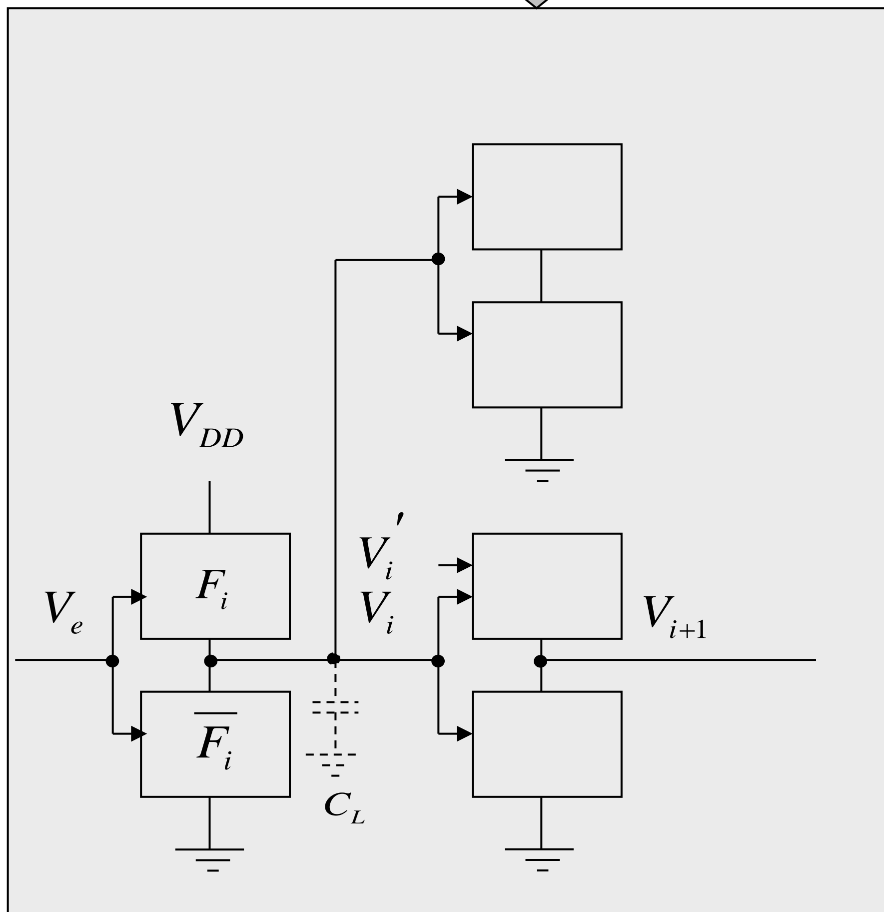
Logic



Memory



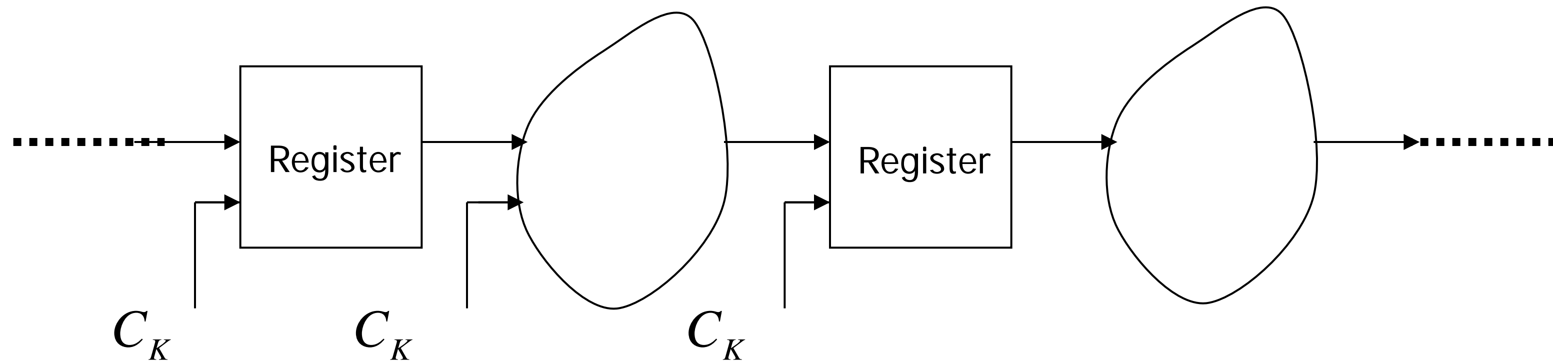




Complementary logic: no current is flowing if states do not change (except leakage)

Realization of a logic function is equivalent to close a serie of switches and to establish a conductive channel between supply and load

Logical depth LD is the maximum of gates in serie between two registers in the pipeline



The activity rate α is the mean probability a gate change of state during the period T

N total number of gates

C_L mean load capacitance

f operating frequency

L_D logical depth

α activity factor

$$f_{\max} = \frac{I_{on}}{L_D \cdot C_L \cdot V_{DD}}$$

$$P_{dyn} = a \cdot N \cdot C_L \cdot V_{DD}^{\;2} \cdot f$$

$$P_{stat} = N \cdot V_{DD} \cdot I_{off}$$

- CMOS: what is necessary to know…
- **Power dissipation: static power and dynamic power**
- Power optimization at component and circuit level
- Power dissipation at architecture level
- Adiabatic and reversible computing

$$P_{total} = P_{active} + P_{standby} =$$

$$= P_{dyn} + P_{short} + P_{leak}$$

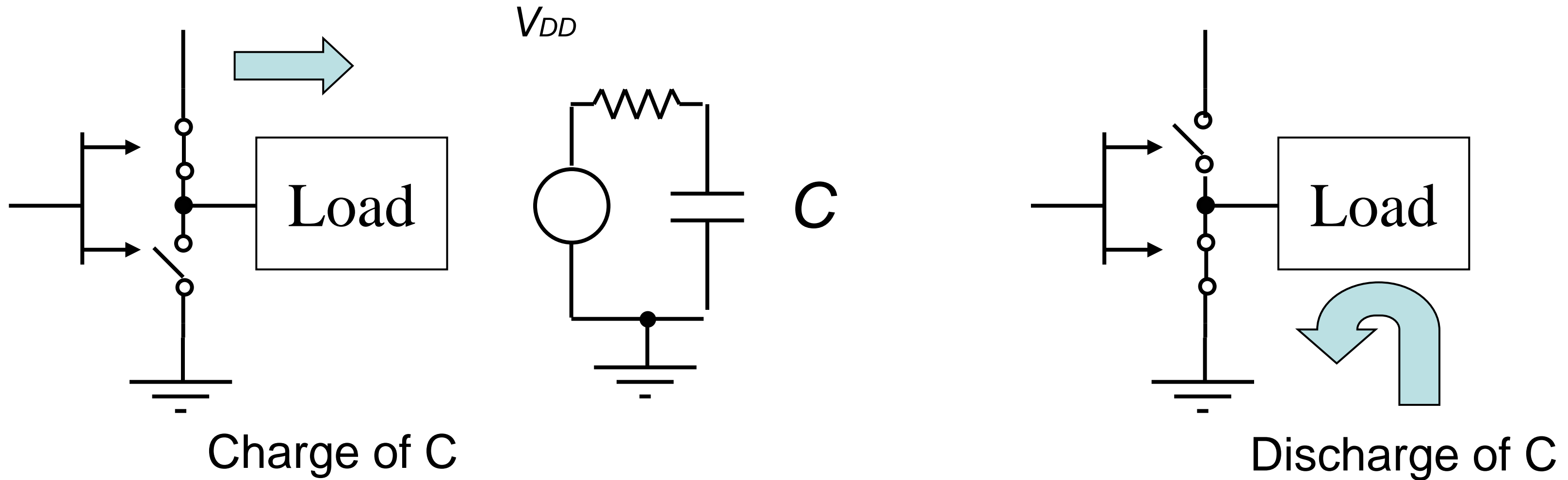
P_{dyn} $= C\,V^2\alpha f$ = dynamic power

= power dissipated due to charging and discharging (switching) of nodes

→ design & technology related

P_{short} = short-circuit power

only during input transitions, there exists a short-circuit current from *Vdd* to ground → design & technology related



$$E_{\text{supply}} = V_{DD} \cdot \int_0^\infty i(t)dt = V_{DD} \cdot Q = CV_{DD}^{\;2}$$

$$Q = CV_{DD}$$

$$E_C = \frac{1}{2} CV_{DD}^{\;2}$$

Dissipated energy

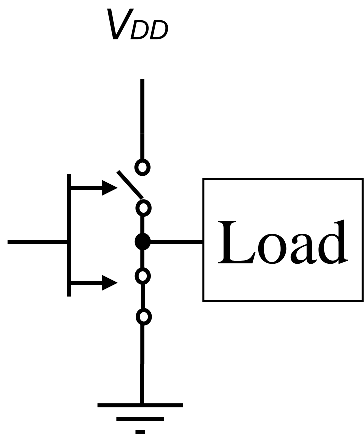
$$E_R = \frac{1}{2} CV_{DD}^{\;2}$$

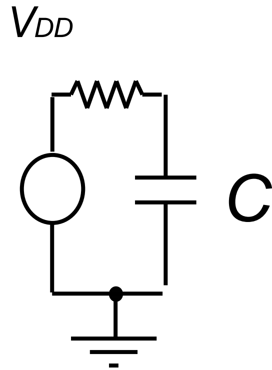
Dissipation independent of *R* (switch resistance) and duration of operation

R may change during transition

Only true if V_{DD} constant (conventional logic)

Leakage power and dynamic power





$$P_{leak} = I_0 \; V_{DD} \exp^{-\frac{V_T}{nV_{th}}} + V_{DD} \; I_t$$

$$P_{dyn} = \alpha \; f \; C \, V_{DD}{}^2$$

$$n = 1 + \frac{C_D}{C_n} \geq 1$$

How to reduce leakage power

The subthreshold current

The tunnel current

$$P_{leak} = N \cdot I_0 \ V_{DD} \exp^{-\frac{V_T}{nV_{th}}} + N \cdot V_{DD} \ I_t$$

To use sleep modes

for circuit or blocks

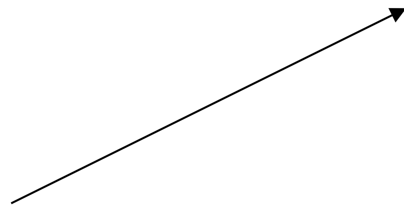
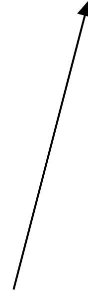
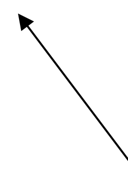
To decrease *n*

To increase threshold voltage

To eliminate tunnel effects

How to reduce dynamic power

$$P_{dyn} = \alpha \, N \, f \, C \, V_{DD}^{\;2}$$

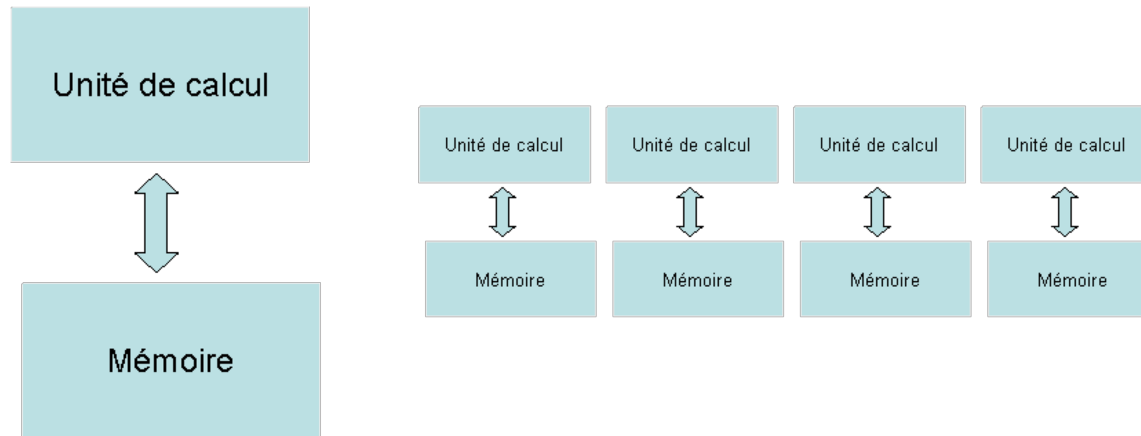
To increase parallelism

To reduce interconnect

To decrease supply voltage

Is it possible to reduce the operating frequency ?

Parallelism is an efficient solution

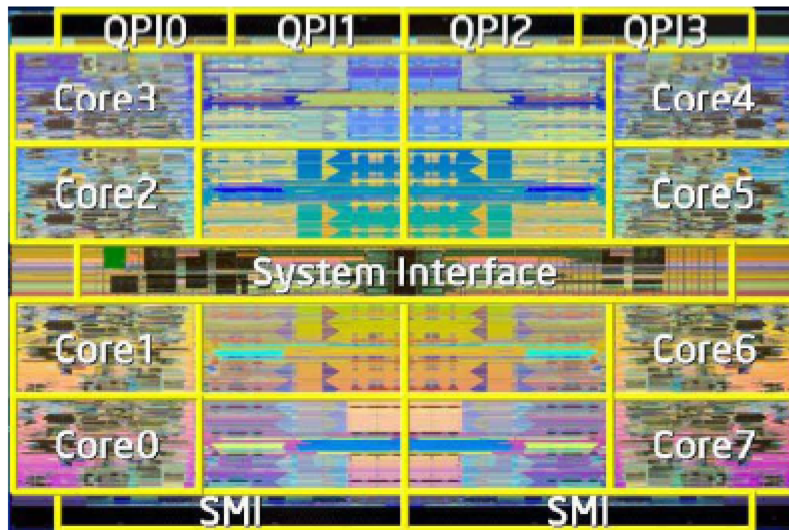


$$P = NfCV^2$$

$$P = 4N\frac{f}{4}\frac{C}{4}\left(\frac{V}{4}\right)^2$$

Today advanced architectures use parallelism but parallelism has limitations

Intel's Nehalem-EX Processor



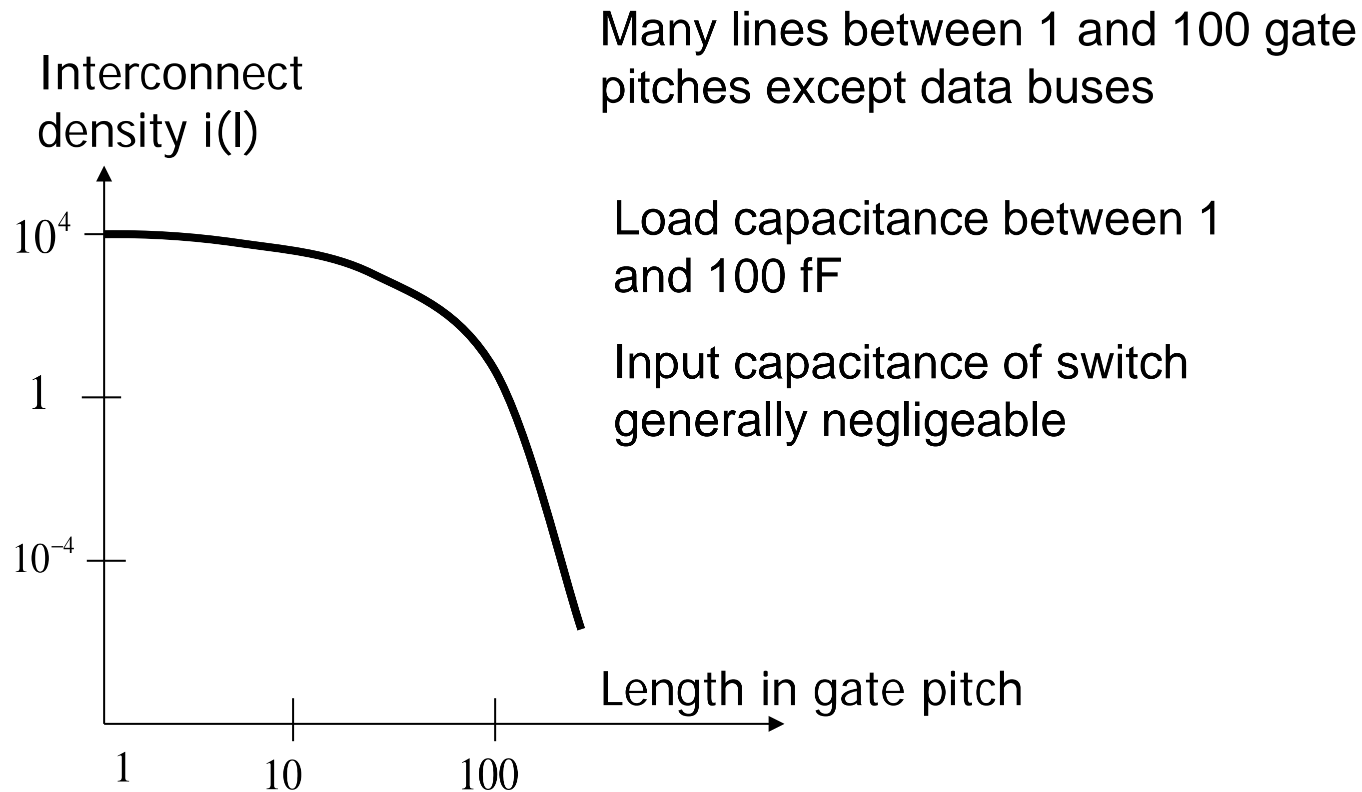
- 45nm process with Hi-K / Metal Gate
- 8 cores, 16 threads
- 24MB L3 cache
- 4 QPI links
- 2.3B transistors
- 130W TDP

- Power reduction techniques:
  - Operate at the lowest possible voltage (0.85V cores, 0.9V cache)
  - Clock and power gate inactive cores and cache slices
  - Multiple voltage and frequency domains, on-die power management unit
  - Extensive use of long channel devices on paths with timing slack

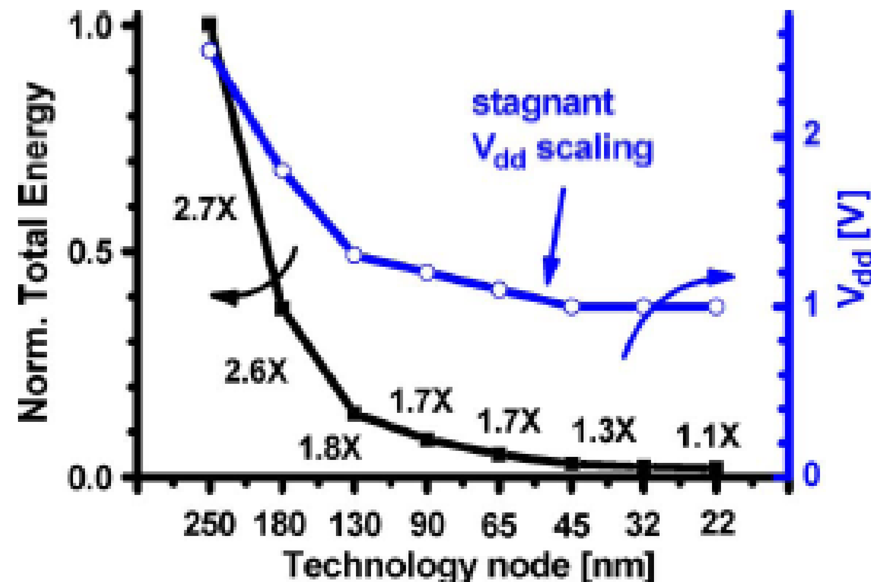
Is it possible to reduce the capacitance ?

	2009	**2012**	**2020**
Métal 1			
C in pF/cm	2	1,8	1,3
RC in ns/mm	1	5	50
Medium			
C in pF/cm	2	1,8	1,3
RC in ns/cm	1	5	50
Global			
C en pF/cm	2,3	2	1,4
RC en ps/cm	11	10	7

Interconnections and load capacitances



Is it possible to reduce the supply voltage ?

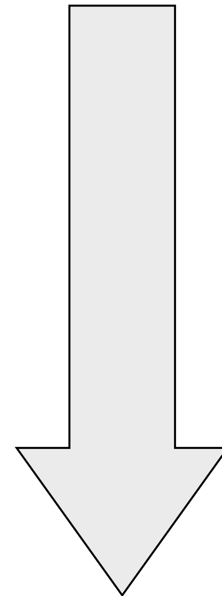


It is not easy to reduce supply voltage…

- CMOS: what is necessary to know
- Power dissipation: static power and dynamic power
- **Power optimization at component and circuit level**
  - **Applications and metrics**
  - **How to reduce supply voltage**
  - **Inerest of steep slope devices**
- Power dissipation at architecture level
- Adiabatic and reversible computing

How to reduce supply voltage, the limits

- 1 Trade-off speed-dissipation
- 2 variability and design constraints
- 3 Cascadability of gates
- 4 Thermodynamical limit



1 The trade-off power-speed

- The power-delay product assigns equal weight to the power and to the delay of a circuit:

$$\text{Power} \cdot \text{Delay} = P_{dyn} \cdot \tau$$

- For circuits for which power has a higher priority than speed, we might give a higher weight to the power than to the delay and the metric becomes:

$$\text{Power} \cdot \text{Energy} = P_{dyn}^{2} \cdot \tau$$

- For high-speed circuits we might give more weight to the delay instead of to the power. Then the metric becomes equal to the energy-delay product:

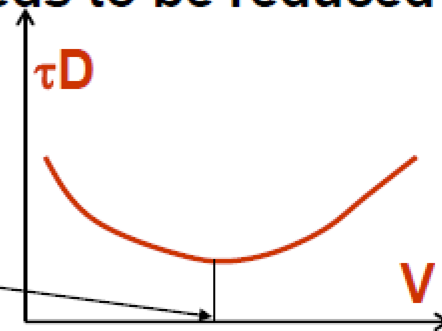
$$\text{Energy} \cdot \text{Delay} = P_{dyn} \cdot \tau^{2}$$

The trade-off power-speed in conventional mode

- very important performance metric is: power-delay product
  - Power = $C\ V^2 \alpha f$
  - delay = $2CV/\beta(V-V_T)^2$

$Q = i\ t = C\ V$
$t = CV/i$ and $i = \beta/2 \bullet (V-V_T)^2$

- to reduce both power and delay, C needs to be reduced
- power-delay product: $\tau D = bV^3/(V-V_T)^2$
- optimum at $\delta\tau D/\delta V = 0 \rightarrow V = 3V_T$

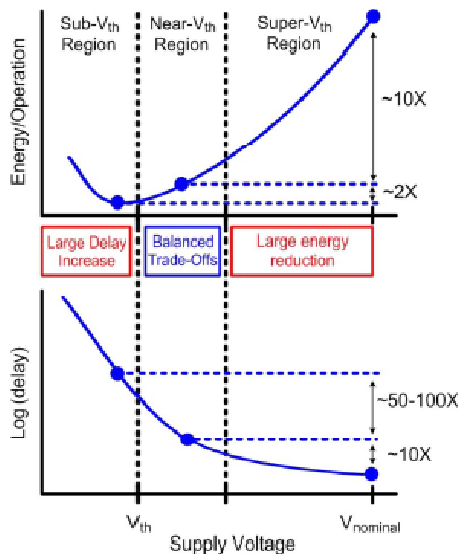


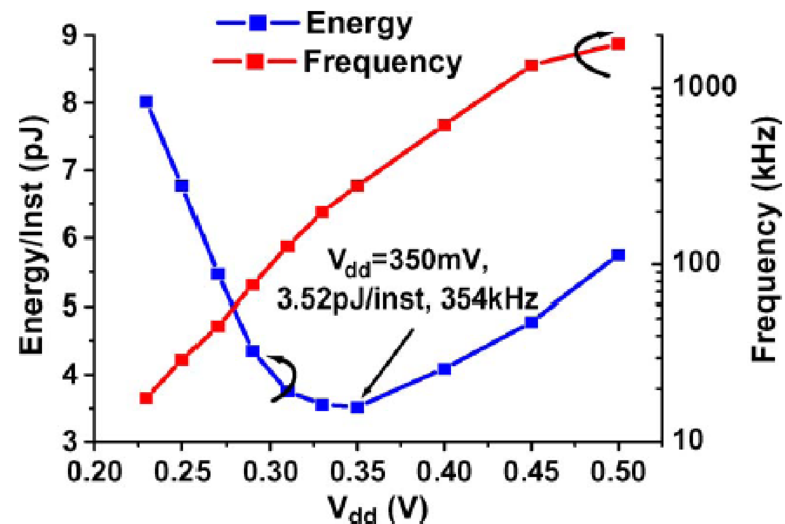
Harry Veendrick IEDM 2009 Short Course •
Low Power / Low Energy Circuits: From Device to System Aspects

The trade-off power-speed in subthreshold mode

$$\tau \approx \frac{V_{DD}}{\left(V_{DD} - V_T\right)^{3/2}}$$

Trade-off speed consumption





Dreslinsky et al proceeding IEEE 2010

To reduce power dissipation low frequency operation is necessary and supply voltage around 0,35 V is optimum for CMOS

- very robust operation with large noise margins
- can operate at Vdd below sum of threshold voltages
- → sub-threshold (logic) operation
- 45nm CMOS (nominal supply: 1.1V) can still operate 80mV
- but, then, only at very low frequencies and with a huge spread:
    - 30mV spread in Vt may lead to 9 times difference in speed, because of huge (leakage) current difference

The mimimum energy operation

B H Calhoun and A chandrakasan: Characterizing and modeling minimum energy operation for subthreshold circuits

$$I_{sub} = I_0 e^{\frac{V_{GS}-V_T}{nV_{th}}}$$

$$t_d = \frac{CV_{DD}}{I_0 e^{\frac{V_{GS}-V_T}{nV_{th}}}}$$

$$E = \alpha \cdot CV_{DD}^{\ 2} + WL_D CV_{DD}^{\ 2} e^{-\frac{V_{DD}}{nV_{th}}}$$

$$V_{DDopt} = nV_{th}\left(2 - lambertW\left(\beta\right)\right)$$

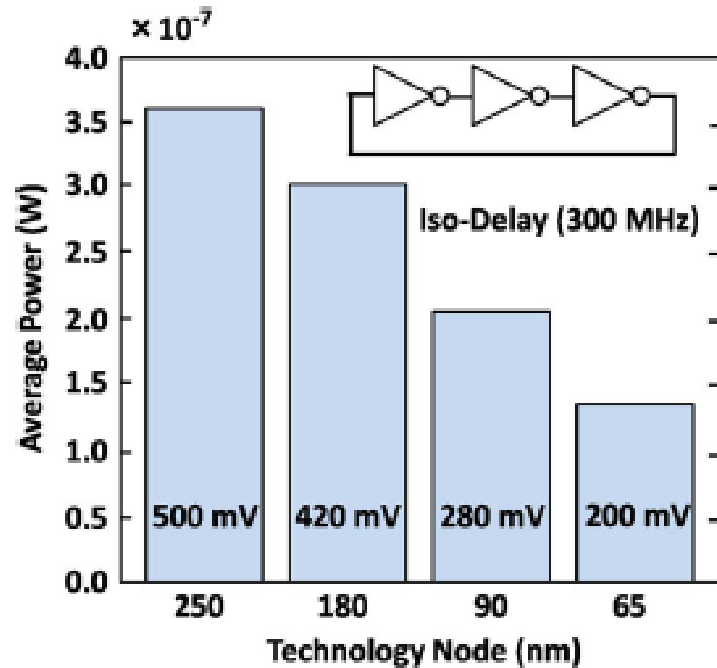
$$\beta = \frac{-2C\alpha}{WCL_D} e^2$$

$$\beta = \frac{-2C\alpha}{WCL_D} e^2 \geq -e^{-1}$$

$$V_{Topt} = V_{DDopt} - nV_{th} \cdot \ln\left(\frac{fCL_D V_{DDopt}}{I_0}\right)$$

$lambertW(x)$ is the solution of $we^w = x$

Decrease of elementary switching energy



Yes but increase of operating gates and variability effects

2 Variability and design constraints

Global analysis necessary including variability and power consumption analysis

$$\tau = k \frac{V_{DD}}{\left(V_{DD} - V_T\right)^{\eta}}$$

$$\eta \approx 1.3$$

$$\Delta\tau = \frac{\tau\left(V_T + \Delta V_{T\max}\right)}{\tau\left(V_T\right)}$$

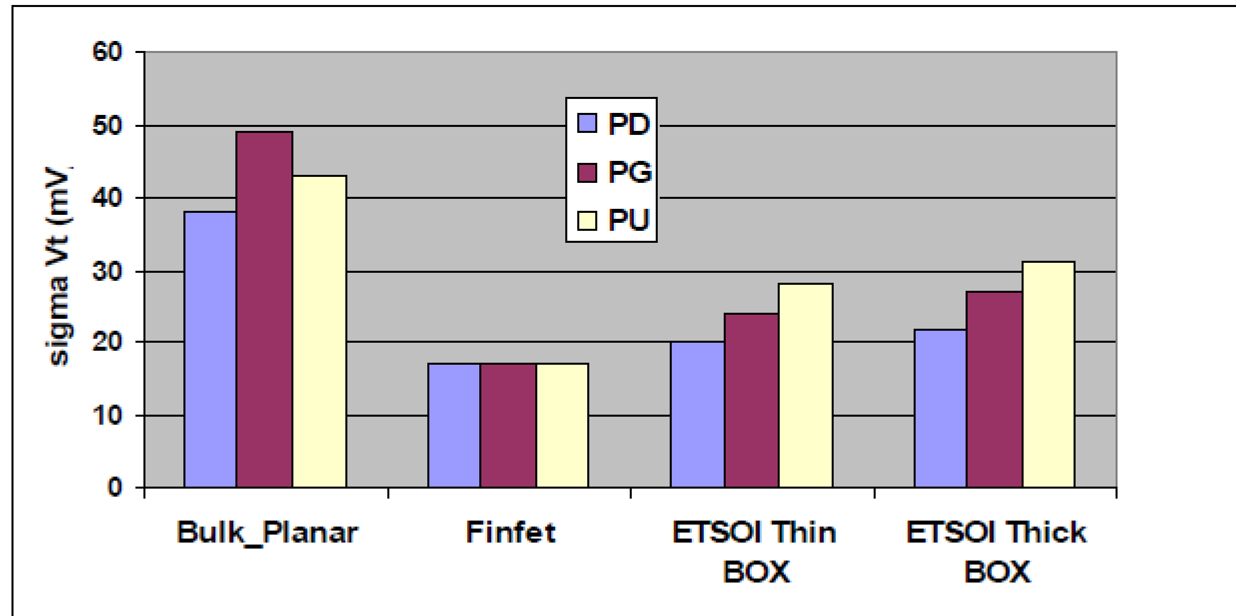
$$\Delta V_{T\max} = \frac{A}{\sqrt{LW}}$$

Law of Pelgrom

$$V_{DD\min} = V_T + \left(1 + \gamma\right)\Delta V_{T\max}$$

$$\gamma = \frac{1}{\Delta\tau^{1/\eta} - 1}$$

Variability and technologies



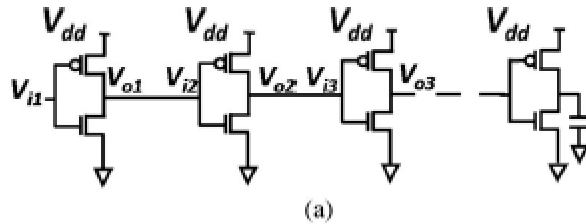
- Dopant fluctuations is dominant component for bulk planar
- Finfet has LER and L_Gate variations primarily
- ETSOI has L_Gate and BOX charge effects

3 The cascadability of gates

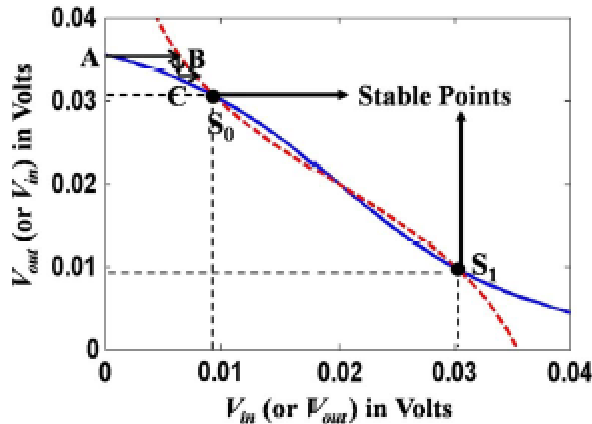
Gupta 2010 proceeding IEEE

The subthreshold regime

$$I = \mu_n V_T^{\,2} e^{\frac{V_{GS}-V_T}{nV_{th}}}\left[1-e^{-\frac{V_{DS}}{mV_{th}}}\right]$$



(a)



A: (V_{i1}, V_{o1}); B: (V_{o2}, V_{i2}); C: (V_{i3}, V_{o3});
S_1: (V_0, V_1); S_0: (V_1, V_0)
(b)

$$n = 1 + \frac{C_D}{C_n}$$

$$V_{th} = \frac{kT}{e}$$

$$m \approx 1$$

The two stable points are the same if

$$V_{DD\min} = 2n\frac{kT}{e} Ln\left(1+\frac{m}{n}\right)$$

4 The fundamental limits

- Boltzmann + Shannon : Minimum switching energy

$$E \succ k_B T \ln 2$$

- Heisenberg : Minimum channel length

$$L \succ \frac{\hbar}{\sqrt{2mE}}$$

- With tunnel effect (Zhirnov-Cavin)

$$E \succ k_B T \ln 2 + \frac{\hbar^2 (\ln 2)^2}{8mL^2}$$

What is the minimum value of VDD- summary

- Trade-off Speed-Power

  200-700 mV (less if low perf)

- Variability and design constraints

  100-300 mV

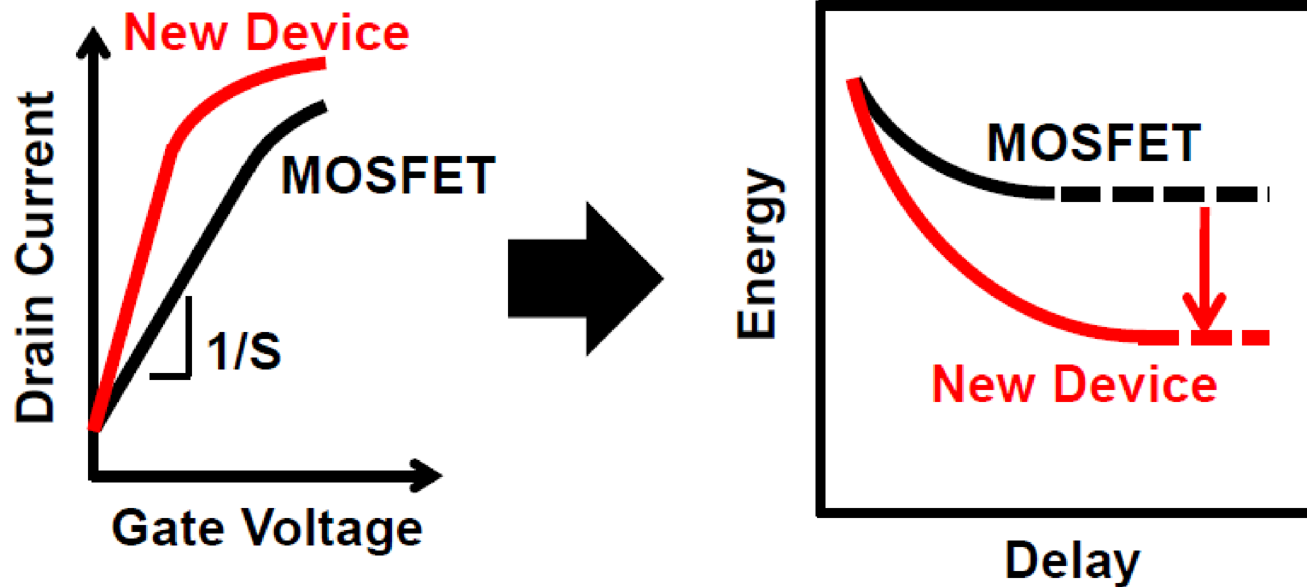
- Cascability of devices

  20-50 mV

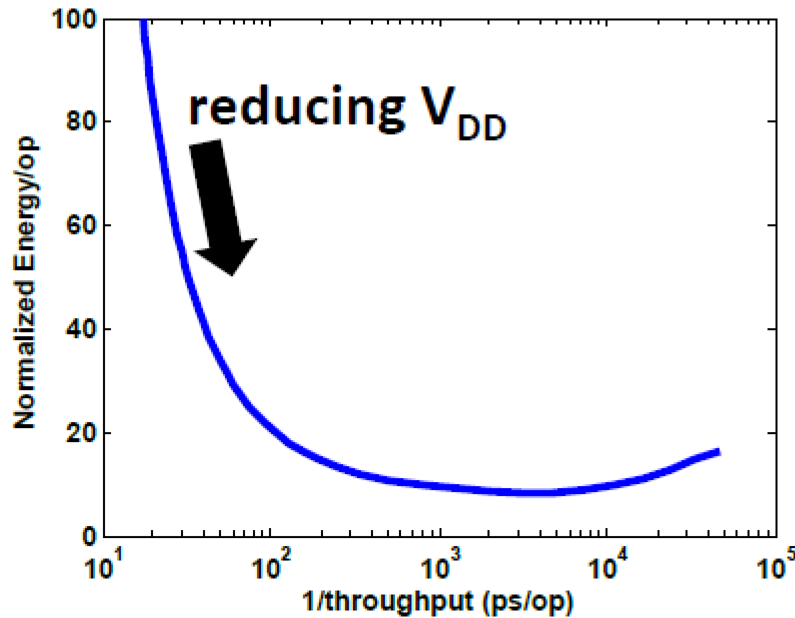
- For very low voltage fundamental limits

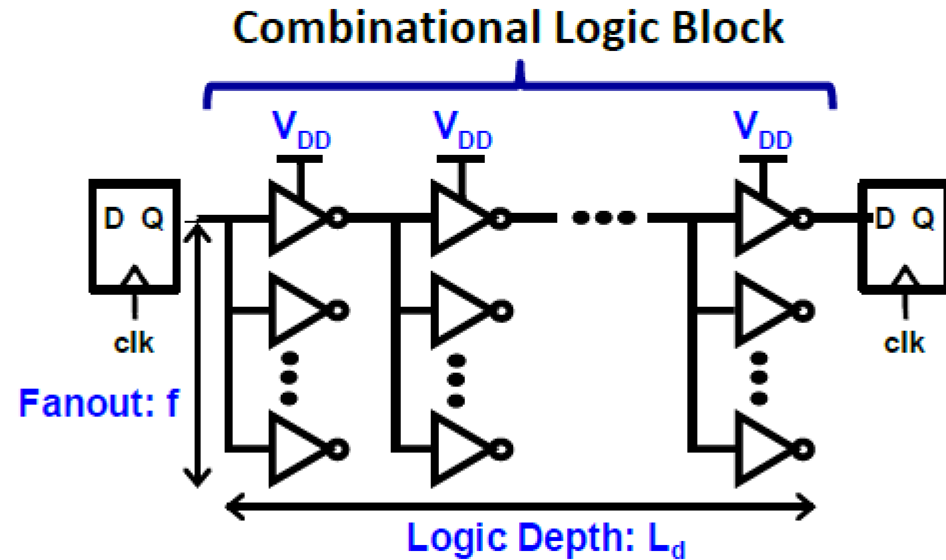
  Below 20 mV towards 2 mV

Interest of steep slope devices ?



Prof. Tsu-Jae King Liu
Workshop on Zero power technologies for Autonomous Smart Systems





Active Energy Passive Energy

$$E_{total} = \alpha L_d f C V_{DD}^2 [1 + (L_d f / 2\alpha)(I_{OFF}/I_{ON})]$$

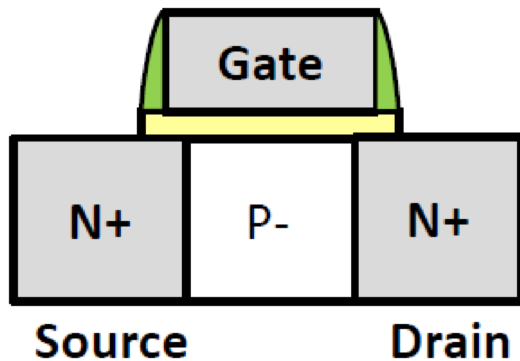
$$t_{delay} = L_d f C V_{DD} / (2 I_{ON})$$

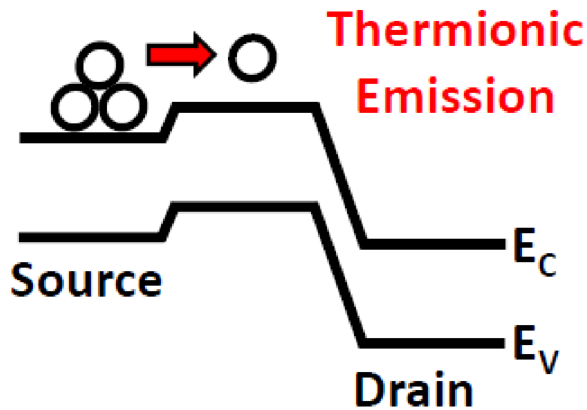
- A lower limit in E/op exists due to transistor OFF-state leakage.

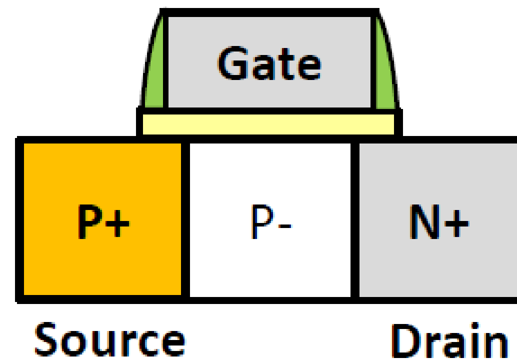
α: Activity Factor L_d: Logic Depth f: Fanout C: Capacitance per Stage

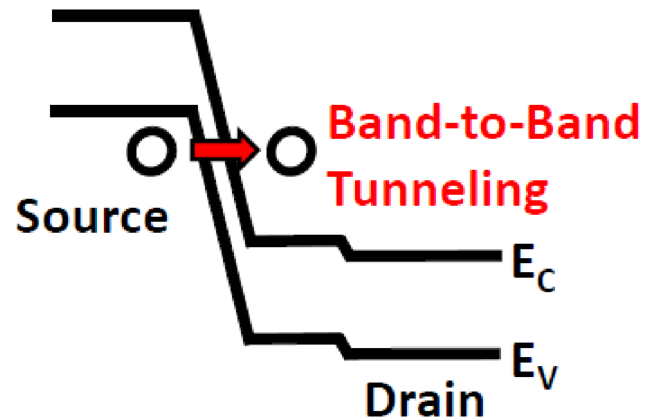
B. Calhoun *et al.*, *IEEE J. Solid State Circuits*, Vol. 50, pp. 1778-1786, 2005

Interest of steep slope devices/ the Tunnel FET









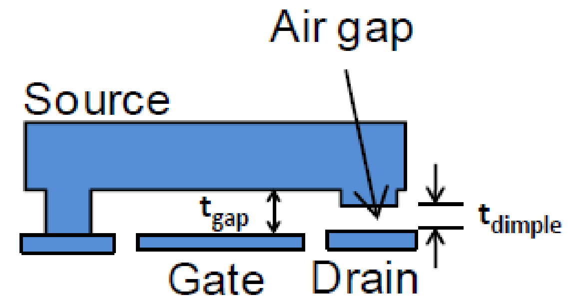
$I_D \propto \exp(qV_{GS}/nkT)$

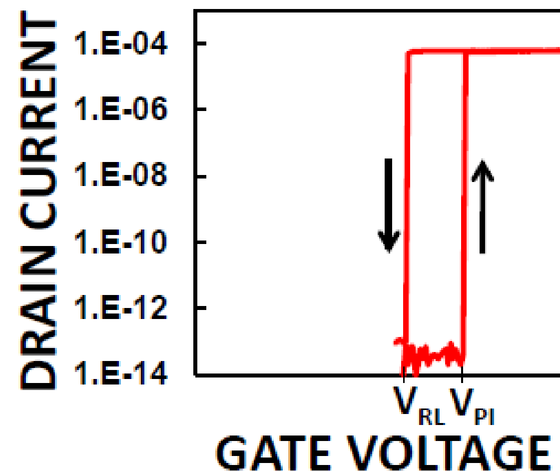
$I_D = AE_S \exp(-B/E_S)$

(E_S = electric field)

Interest of steep slope devices/ the nanomechanical relay

- **Zero off-state leakage**
  → zero leakage energy
- **Abrupt switching behavior**
  → allows for aggressive V_{DD} scaling (ultra-low dynamic energy)





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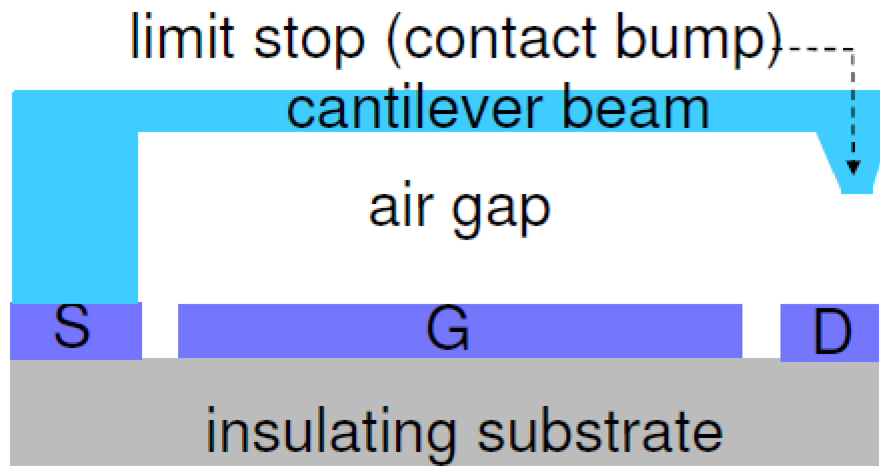
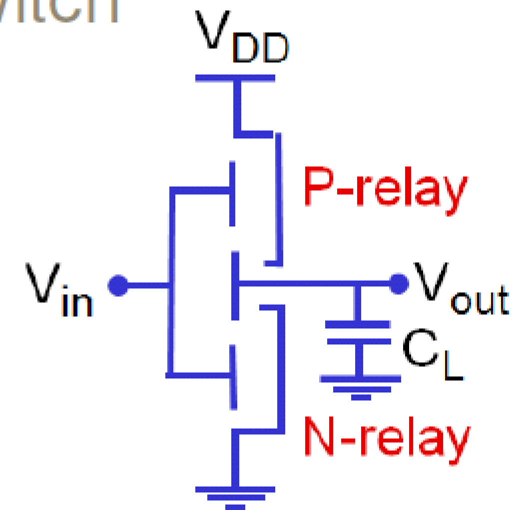
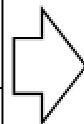
Nano-Electro-Mechanical (NEM) Switch





V_{DD}	1.5 V
V_{pi}	1 V
g_0, h	10 nm
L	~250 nm
W	100 nm

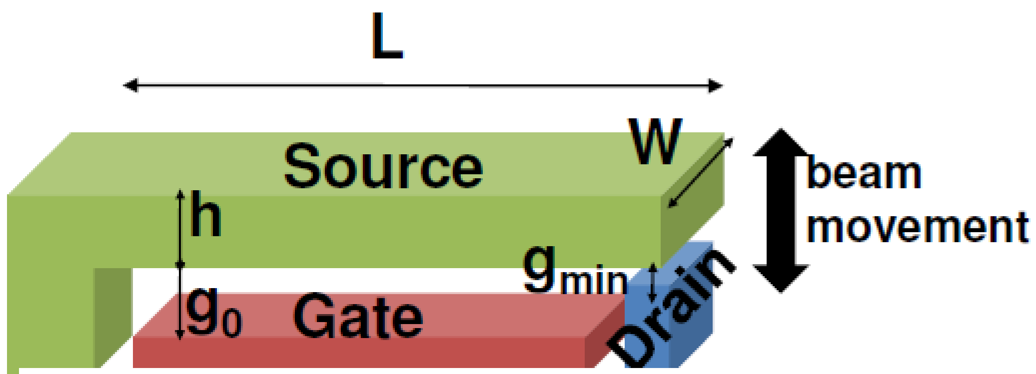


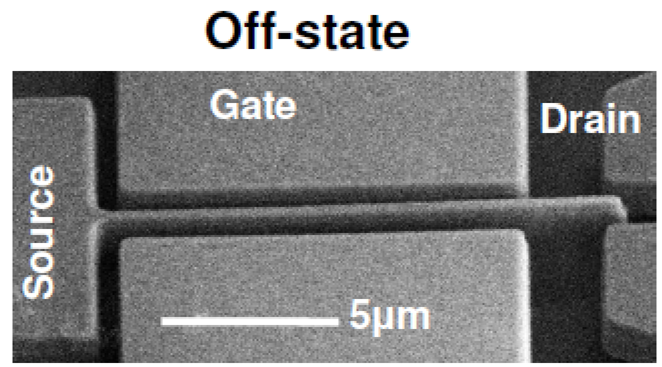
Simple NEM relay

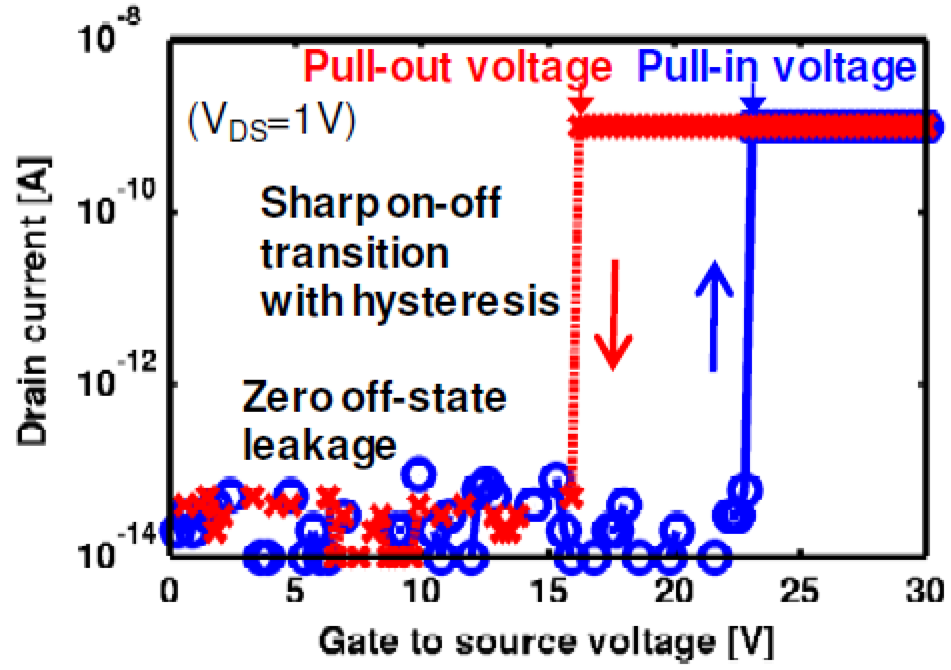
Static Power	'Zero'	
Switching Delay	1 nsec (Si)	
Switching Energy	0.08 fJ (Si)	
Inverter Area	0.03 µm^2	

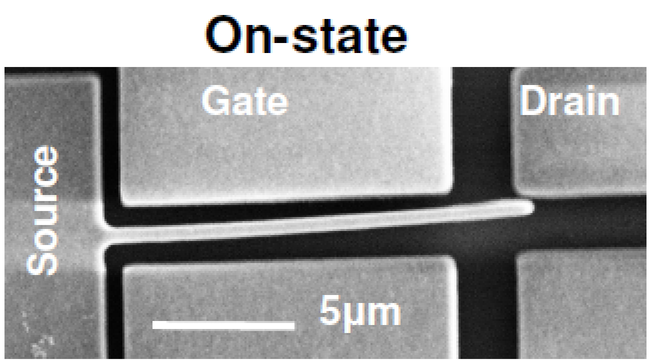
K. Akarvardar, D. Elata, R. Parsa, G. C. Wan, K. Yoo, J. Provine, P. Peumans, R. T. Howe, H.-S. P. Wong, "Design Considerations for Complementary Nanoelectromechanical Logic Gates," *IEEE International Electron Devices Meeting (IEDM)*, p. 299, December 10 – 12, Washington, D.C., 2007.

Nanoelectromechanical (NEM) Relay







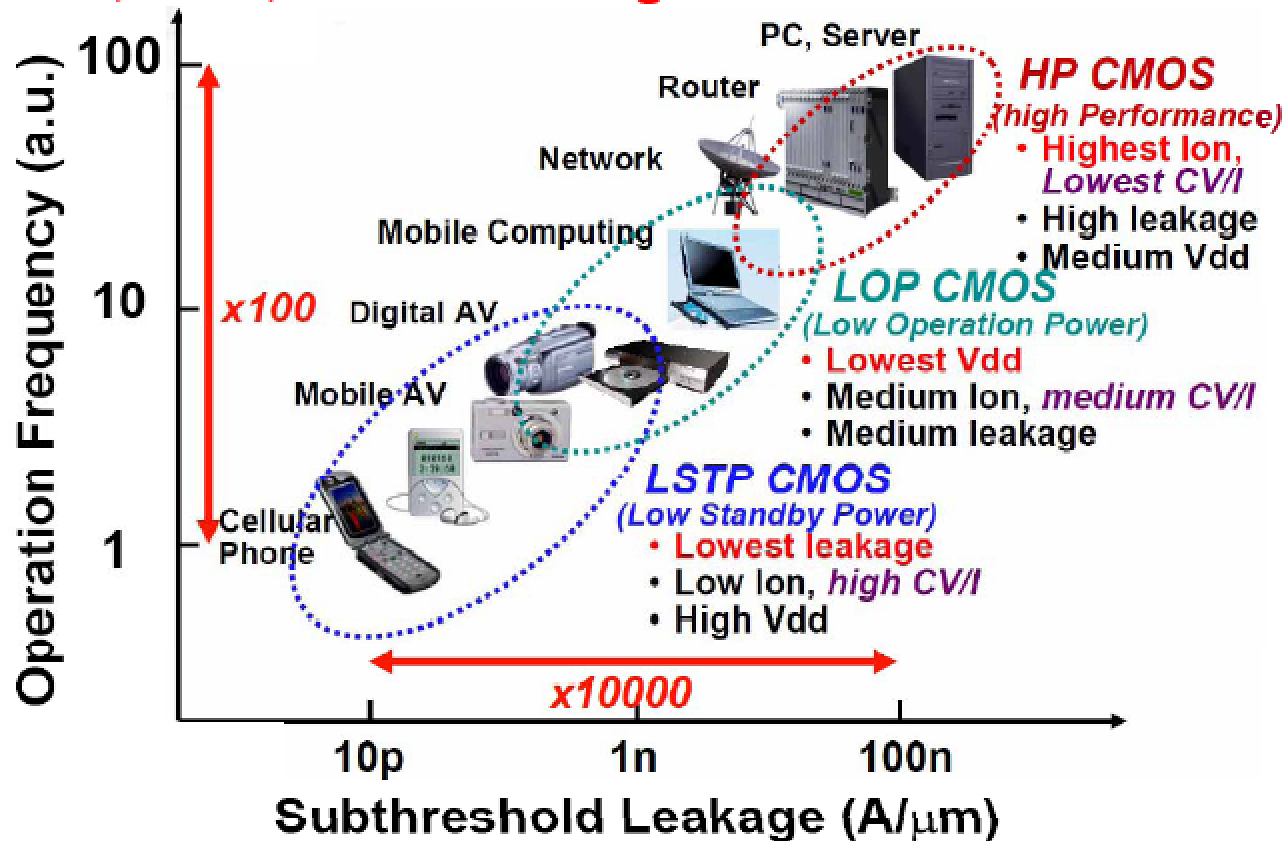


S. Chong ...H.-S. P. Wong, "Nanoelectromechanical (NEM) Relays Integrated with CMOS SRAM for Improved Stability and Low Leakage," *ICCAD* 2009.

- **NEM switches have several potential advantages compared with nanoscale CMOS transistors:**
  - low power supply (100 mV)
  - high on current
  - ‘zero’ leakage
  - ‘infinite’ subthreshold slope
  - high temperature operation
  - radiation-hard operation
  - compatible with other substrates … glass, plastics

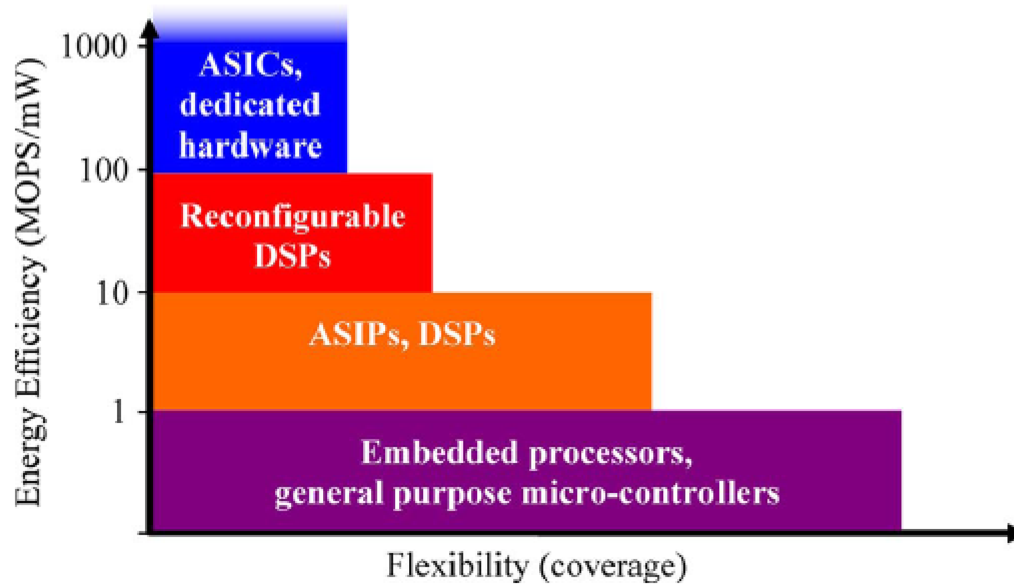
- **… and “just a few” problems:**
  - reliability (stiction, contact degradation, wear, …)
  - slow speed

- CMOS: what is necessary to know…
- Power dissipation: static power and dynamic power
- Power optimization at component and circuit level
- **Power dissipation at architecture level**
- Adiabatic and reversible computing



HP, LOP, LSTP for Logic CMOS
Operation Frequency (a.u.)
100
10
1
x100
PC, Server
Router
Network
Mobile Computing
Digital AV
Mobile AV
Cellular Phone
HP CMOS
(high Performance)
• Highest Ion, Lowest CV/I
• High leakage
• Medium Vdd
LOP CMOS
(Low Operation Power)
• Lowest Vdd
• Medium Ion, medium CV/I
• Medium leakage
LSTP CMOS
(Low Standby Power)
• Lowest leakage
• Low Ion, high CV/I
• High Vdd
x10000
10p
1n
100n
Subthreshold Leakage (A/μm)
Source: 2007 ITRS Winter Public Conf.
1

Trade-off flexibility-power



With an ASIC a factor 100 is possible for power reduction

Optimization of voltage and frequency

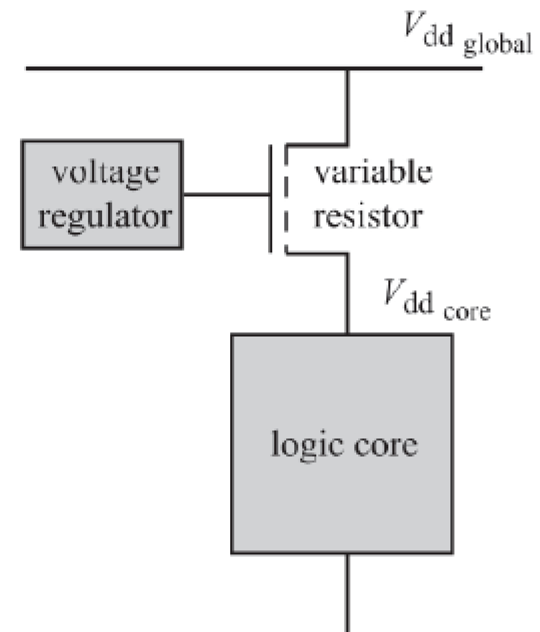
dynamic voltage and frequency scaling (DVFS)

• dynamically adjusting the voltage to the performance needs

• requires on- or off-chip voltage regulator

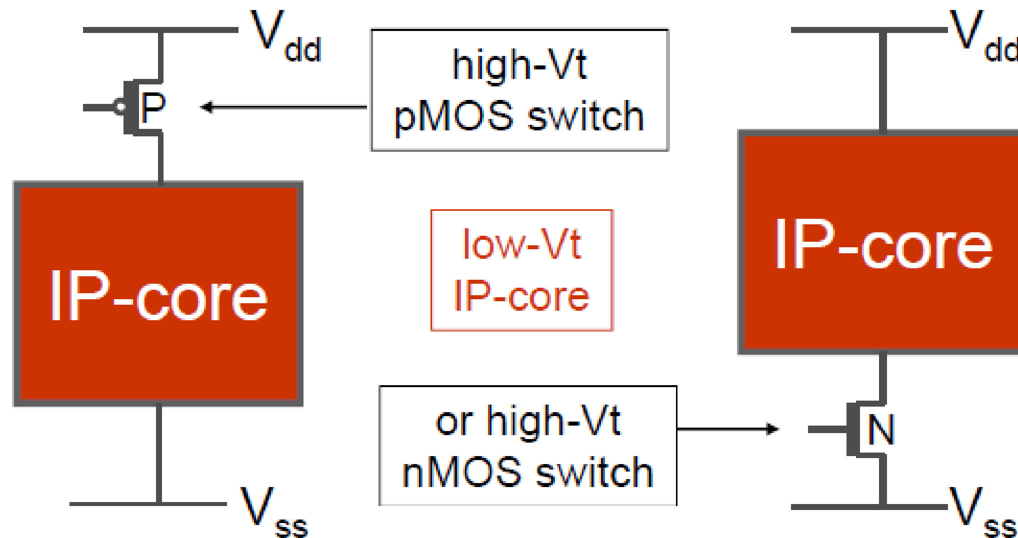
• varying the resistance of a big transistor between the core and the supply voltage

• but power reduces only linearly with the V_{ddcore} instead of quadratically, since part of the power saving in the core is now consumed in the variable resistor.



Optimization of Threshold voltages

- **multiple V_t concept: HVt power switches**
  - switch off low-V_t core with high-V_t transistors (high-V_t power switches)
  - disadvantages: core flip-flops lose their states → multi-supply flip-flops

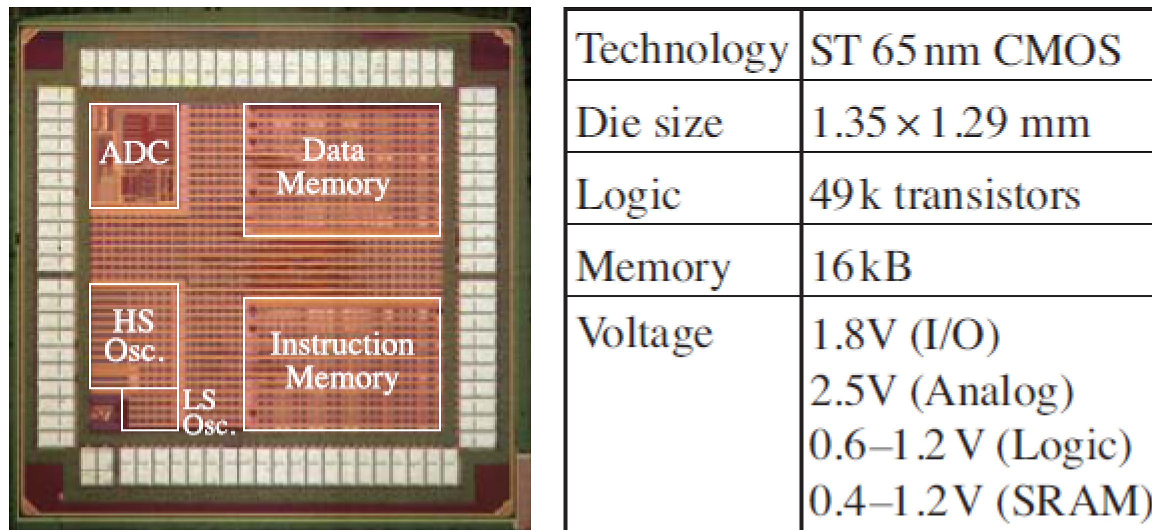


Optimization of SRAMS

- **reduce supply voltage of memory array in standby mode**
  - memory operation is very critical wrt supply voltage
  - but in standby mode only data retention is required
  - can be done at (somewhat) lower voltages
  - use of 7 or 8 transistor cells may also support low-standby voltage

- **use high-Vt transistors in the memory cells**
  - most transistors of an SoC are in the memory (often > 80%)
  - so, memories relatively contribute most to the standby power
  - HVt transistors in the cells will greatly reduce standby power

A low power processor



Technology	ST 65 nm CMOS
Die size	1.35 × 1.29 mm
Logic	49 k transistors
Memory	16 kB
Voltage	1.8V (I/O) 2.5V (Analog) 0.6–1.2 V (Logic) 0.4–1.2V (SRAM)

Fig. 5.   Chip photomicrograph and design statistics.

A low power processor

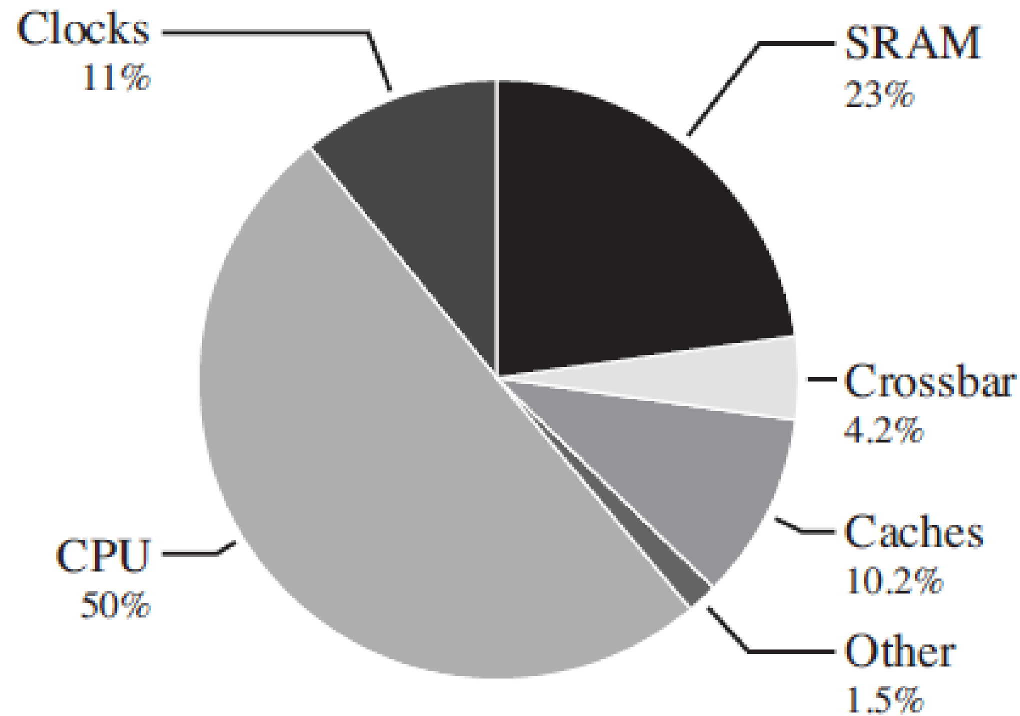
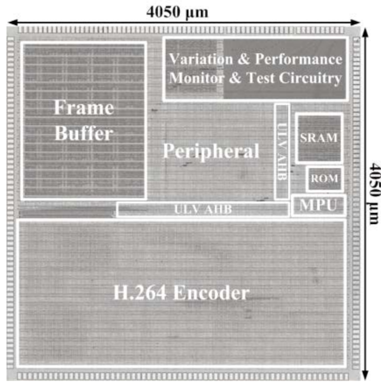


Fig. 7. Breakdown of digital power consumption by module at 0.6 V (SRAM array voltage 0.4 V).

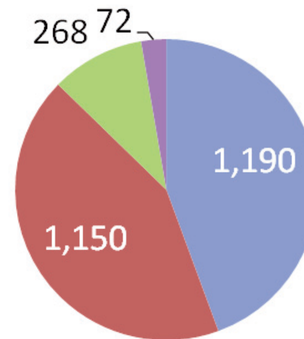
A low power SOC



H.264 encoder,

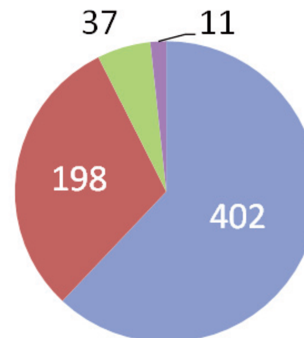
65nm low-power technology,

1.0V, down to 0.57nJ/pixel

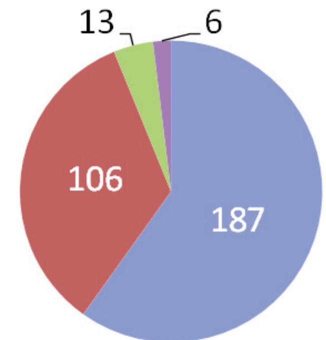


Dynamic (Logic)
Leakage (Logic)
Dynamic (Memory)
Leakage (Memory)

V_{DD}=1.0V
Total power = 2.68mW

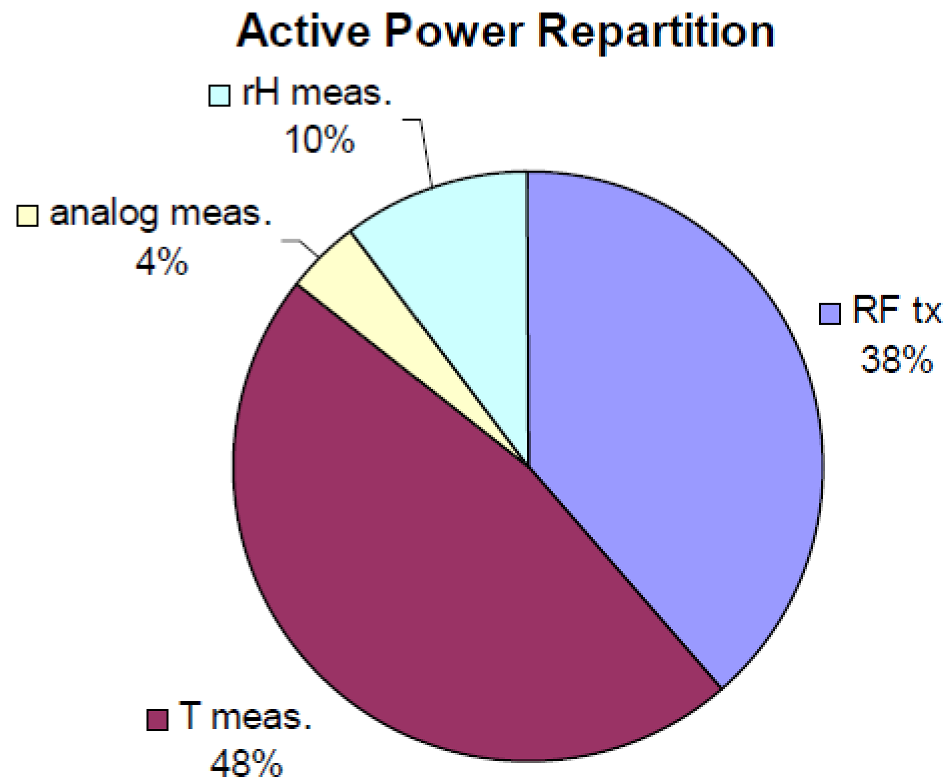


V_{DD}=0.6V
Total power = 648µW



V_{DD}=0.48V
Total power = 312µW

Example of an autonomous sensor for energy efficiency in building



Example of an autonomous sensor for energy efficiency in building

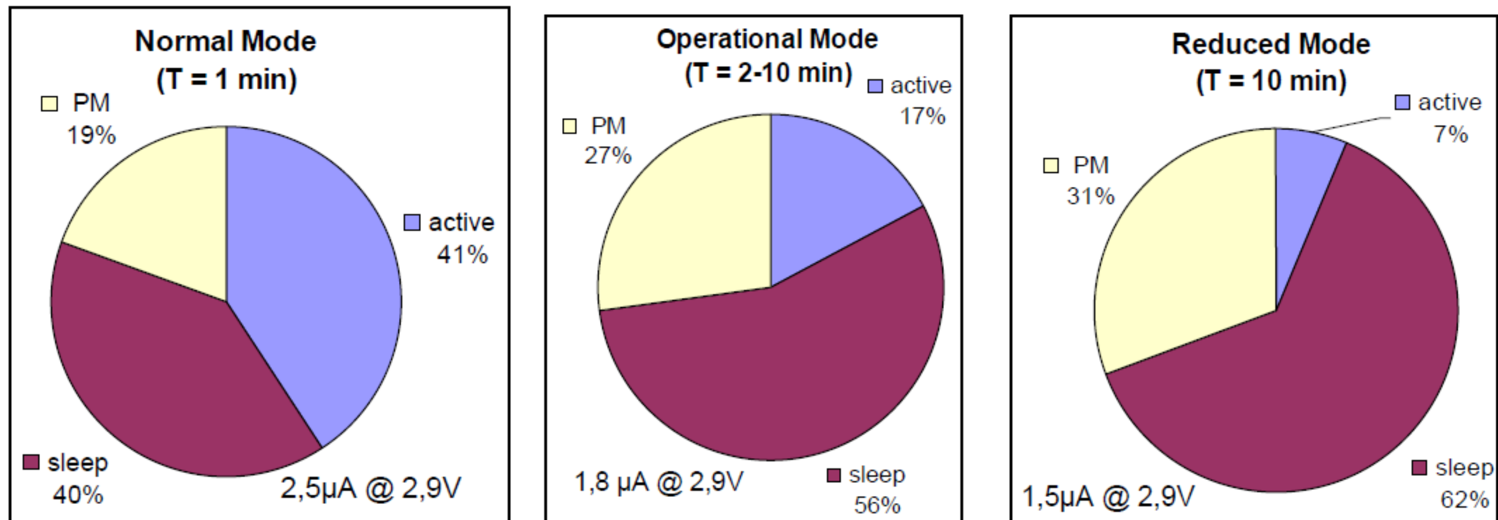
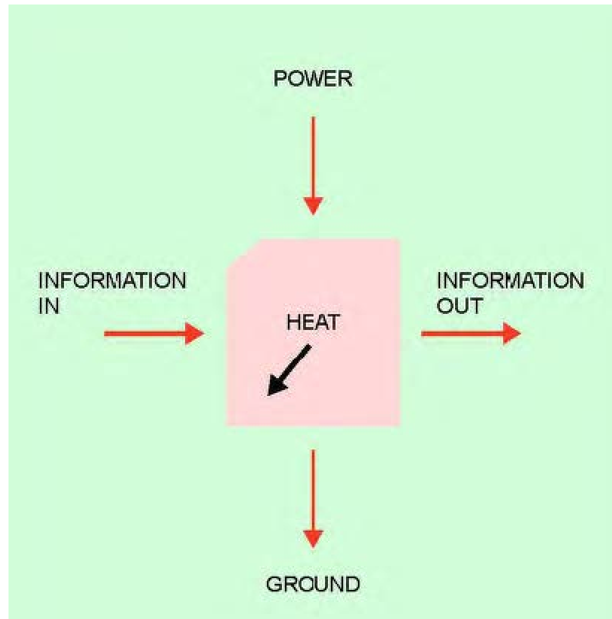


Figure 22 : Current consumption repartition in function of demonstrator operating mode

- **CMOS: what is necessary to know…**
- Power dissipation: static power and dynamic power
- Power optimization at component and circuit level
- Power dissipation at architecture level
- **Adiabatic and reversible computing**

Adiabatic logic	**Reversible logic**
How to charge and discharge a capacitance with minimum energy dissipation *To work at constant current*	How to take into account Landauer principle in order to minimize energy dissipation *To use only reversible logic*

Information and heat dissipation



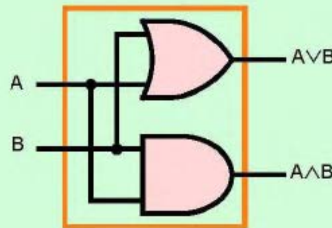
$$\Delta Q = T\Delta S$$

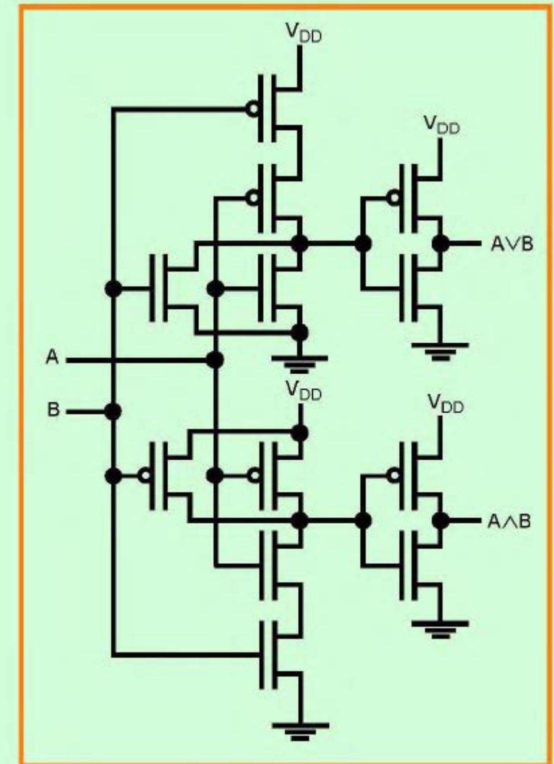
$$\Delta H = \Delta\left(-\sum_i p_i \ln_2 p_i\right)$$

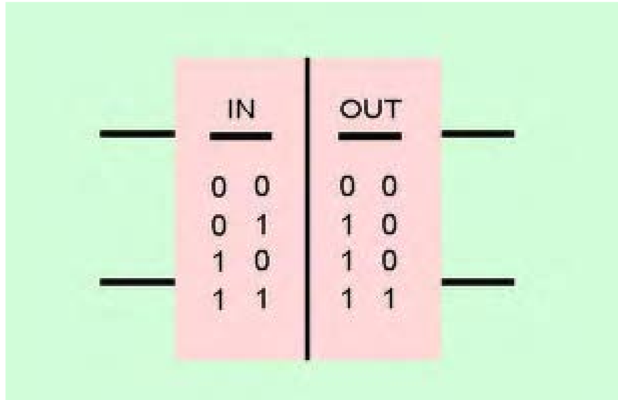
$$\Delta S = k\Delta H$$

Information and heat dissipation

IN		OUT	
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1







$$H_{in} = -\sum_{states} p_{state}\log_2 p_{state} = -4\times\frac{1}{4}\log_2\frac{1}{4} = 2$$

$$H_{out} = -2\times\frac{1}{4}\log_2\frac{1}{4} - \frac{1}{2}\log_2\frac{1}{2} = \frac{3}{2}$$

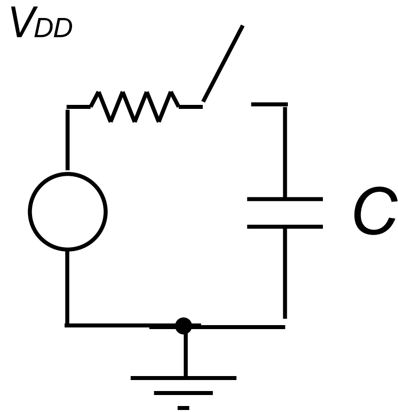
An example of non reversible gate

Impossible to guess inputs from outputs

Input			Output		
C_1	C_2	T	C_1	C_2	T
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

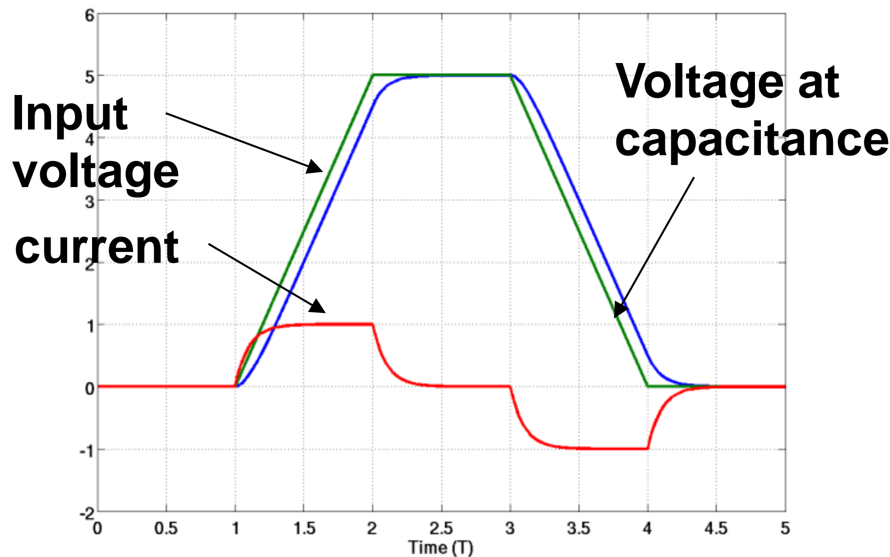
An example of a reversible gate: the Toffoli Gate

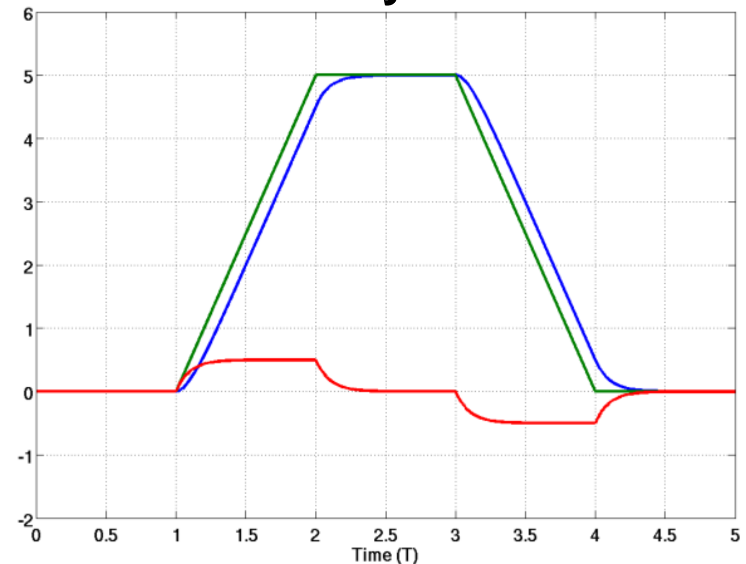
The adiabatic charge of a capacitance



Not an abrupt variation but a linear variation is applied to the capacitor

If *RC* is small compared to the duration *T* of the ramp, charge-discharge currents and Joule dissipation are small





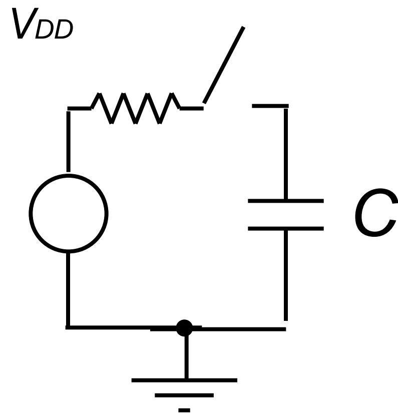
1) Conventional

$$E_{a\lim} = V_{DD} \cdot \int_0^{\infty} i(t)dt = V_{DD} \cdot Q = CV_{DD}^{\ 2}$$

$$Q = CV_{DD}$$

$$E_C = \frac{1}{2} CV_{DD}^{\ 2}$$

$$E_R = \frac{1}{2} CV_{DD}^{\ 2}$$



Only true if V_{DD} does not vary with time

2) Adiabatic

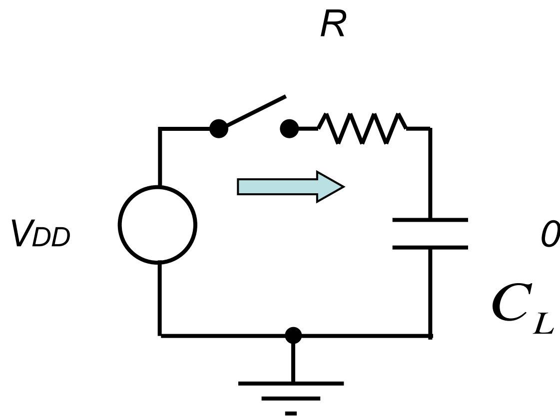
$$Q = CV_{DD}$$

$$i = \frac{Q}{T}$$

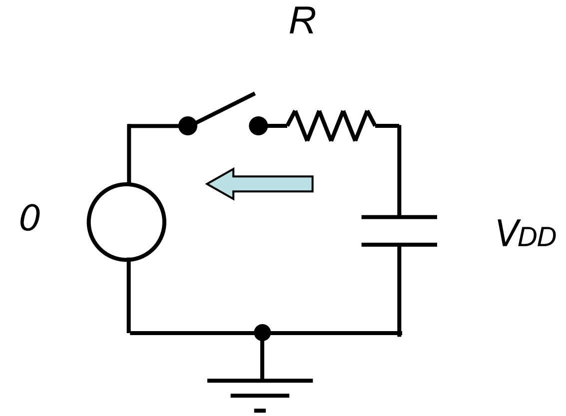
$$E_R = Ri^2T = R\frac{Q^2}{T^2}T = \frac{RC}{T} CV_{DD}^{\ 2}$$

Only true if i does not vary with time

Charge of CL



Discharge of CL



$$E_{dissipée} = \frac{RC_L}{T} C_L V_{DD}^{\ 2} \qquad i = \frac{C_L \cdot V_{DD}}{T}$$

- **Charge is at constant current during T and voltage at the end is VDD**
- **Energy savings are huge is *RC/T* is small**
- **It is also necessary to recover energy and specific supply modules are requested**

RC charging at minimum dissipation theory

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Optimal Charging of Capacitors
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The input voltage for a given optimality criterion is computed by The methods used are variational calculus and Pontrjagin's maximum principle. This material is well established in mathematics and control and we refer to the literature for details [3]. The procedure to compute the input voltage $v_i(t)$ is the following.

1) Given the dynamical system

$$\frac{dx}{dt} = a(x) + b(x)v(t)$$

with a, b, x scalars.

2) Define the Hamilton function

$$H(\lambda, x, v, t) = -L(x, v) + \lambda(a(x) + b(x)v(t)). \quad (1)$$

The time integral of $-L(x, v)$ is to be minimized. For the case of loss minimization it measures the power in the resistor, in our case, $L(x, v) = -(v_i(t) - v_c(t))^2/R$. If minimal time charging is to be achieved, the function is simply one.

3) Solve

$$\frac{\partial H}{\partial v_i} = 0 \quad (2)$$

for v_i.

4) Solve

$$\frac{d\lambda}{dt} = -\frac{\partial H}{\partial x} \quad (3a)$$

$$\frac{dx}{dt} = \frac{\partial H}{\partial \lambda} \quad (3b)$$

$$H = \frac{(v_i(t) - v_C(t))^2}{R} + \lambda(t)\frac{1}{\tau}(v_i(t) - v_C(t)). \quad (7)$$

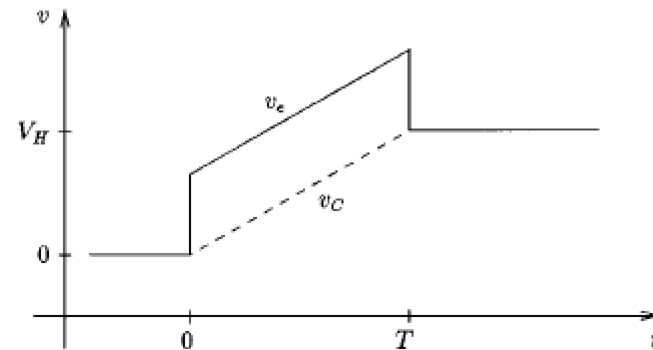
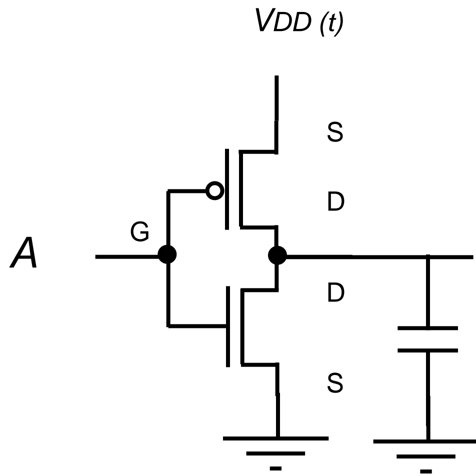
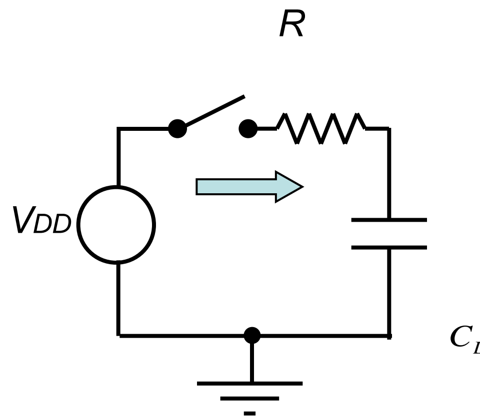


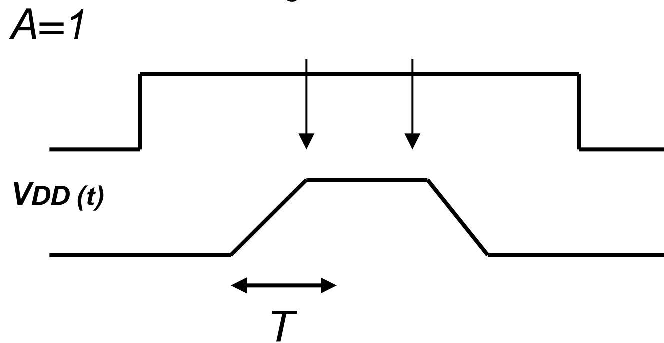
Fig. 3. Input signals for maximum efficiency of linear circuit.

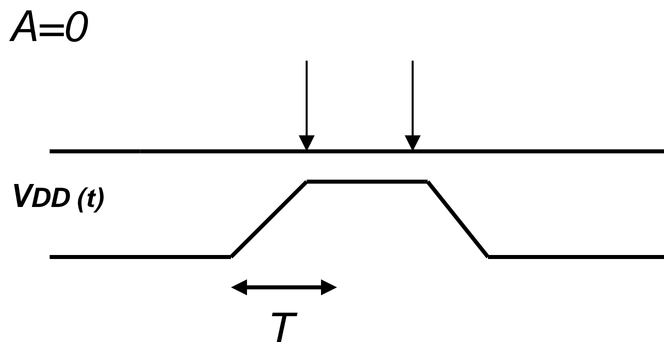




Charge of C_L

Logic state evaluation





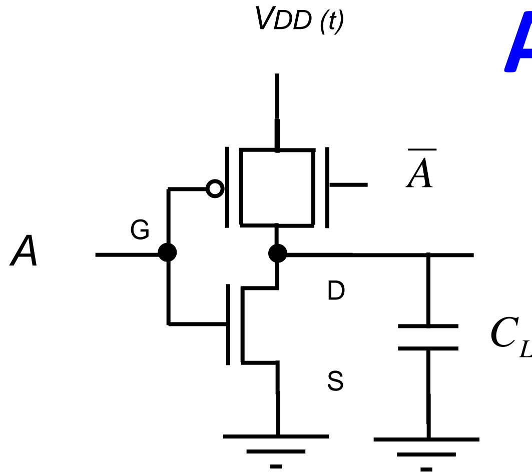
Input voltage stable during transition otherwise non adiabatic dissipation

PMOS is on only if VDD greater than VT

Non adiabatic dissipation

$$\frac{1}{2} C_L {V_T}^2$$

A more efficient solution



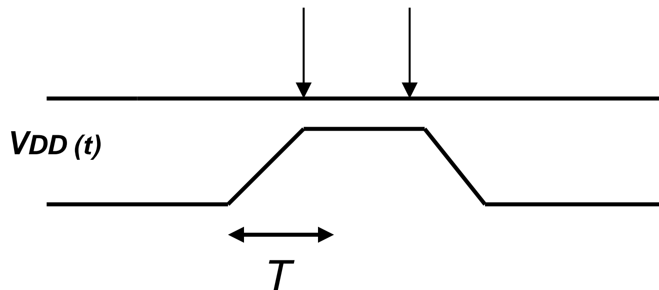
$$I_{Dn} = \frac{W_n}{L_n}\mu_n C'_{ox}\left[(V_{GSn} - V_{Tn})V_{DS} - V_{DS}{}^2\right]$$

$$I_{Dp} = \frac{W_p}{L_p}\mu_p C'_{ox}\left[(V_{SGp} - V_{Tp})V_{SD} - V_{SD}{}^2\right]$$

$$g_{on} = \frac{\partial I_{Dn}}{\partial V_{DS}} = \frac{W_n}{L_n}\mu_n C'_{ox}(V_{GSn} - V_{Tn}) = \frac{W_n}{L_n}\mu_n C'_{ox}(V_{DD} - V_{DD}(t) - V_{Tn})$$

$$g_{op} = \frac{\partial I_{Dp}}{\partial V_{DS}} = \frac{W_p}{L_p}\mu_p C'_{ox}(V_{GSn} - V_{Tn}) = \frac{W_p}{L_p}\mu_p C'_{ox}(V_{DD}(t) - V_{Tp})$$

A=0



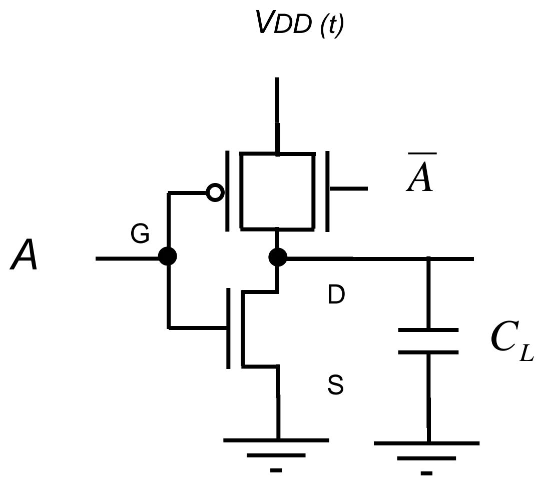
VDS close to 0

we consider $\frac{W_n}{L_n}\mu_n C'_{ox} = \frac{W_p}{L_p}\mu_p C'_{ox}$

$$g = \frac{W_n}{L_n}\mu_n C'_{ox}(V_{DD} - 2V_T)$$

W/L =1 45 nm 1/g=2500 Ω

W/L =10 45 nm 1/g=250 Ω



$$E_{dyn} = \frac{RC_L}{T} C_L V_{DD}{}^2 = \frac{L^2}{C_n} \frac{C_L{}^2}{\mu_n} \frac{V_{DD}{}^2}{\left(V_{DD} - 2V_T\right)} \frac{1}{T}$$

$$avec \quad C_n = C'_{ox} WL$$

With leakage power

$$E_{stat} = \frac{\mu_n C_n}{L^2} V_{th}{}^2 e^{-\frac{V_T}{nV_{th}}} V_{DD} T$$

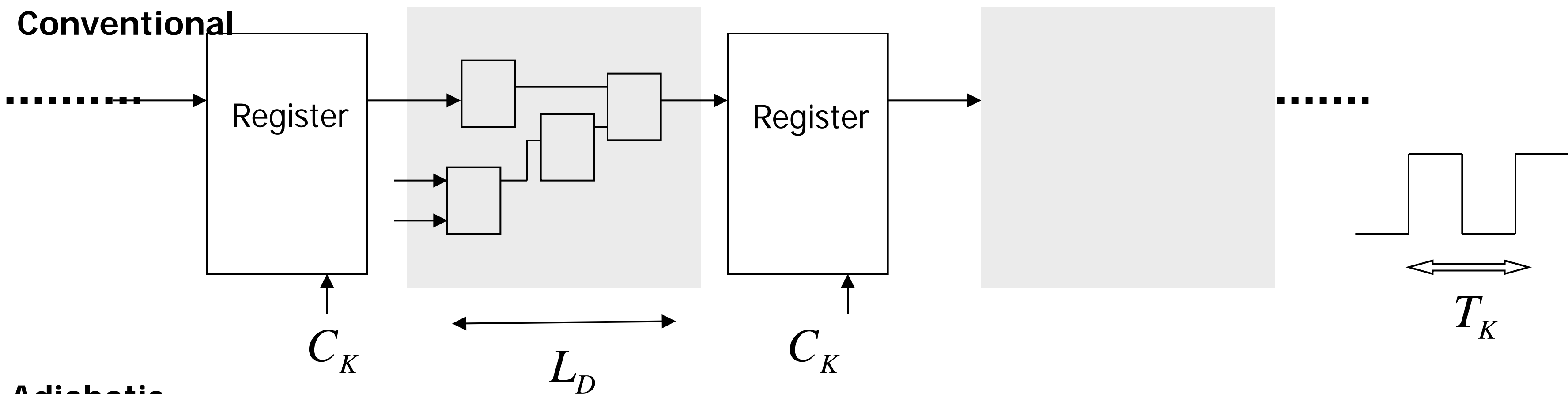
$$avec \quad V_{th} = \frac{kT}{e}$$

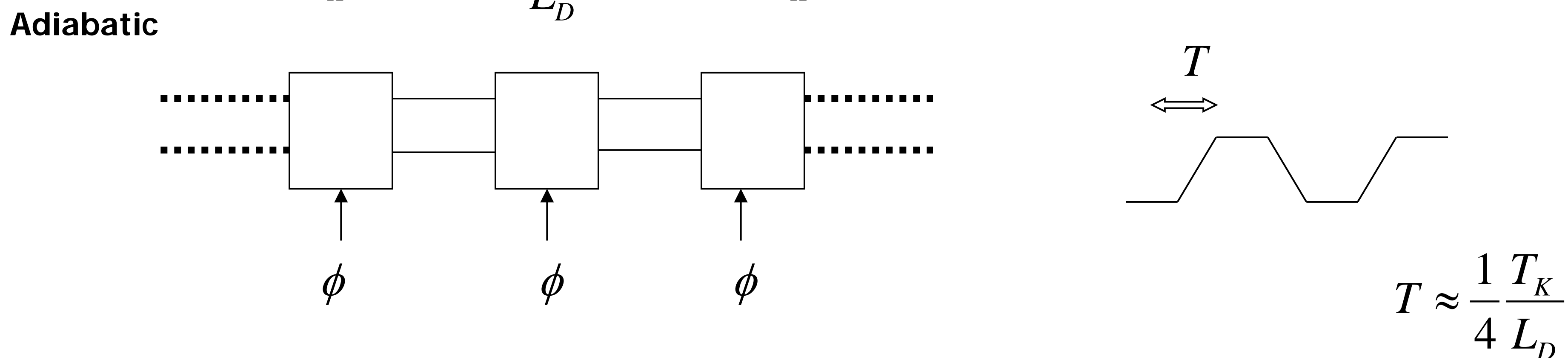
$$n = 1 + \frac{C_D}{C_n}$$

$$E = a \frac{L^2}{C_n} \frac{C_L{}^2}{\mu_n} \frac{V_{DD}{}^2}{\left(V_{DD} - 2V_T\right)} \frac{1}{T} + \frac{\mu_n C_n}{L^2} V_{th}{}^2 e^{-\frac{V_T}{nV_{th}}} V_{DD} T$$

Activity factor =1

in adiabatic mode





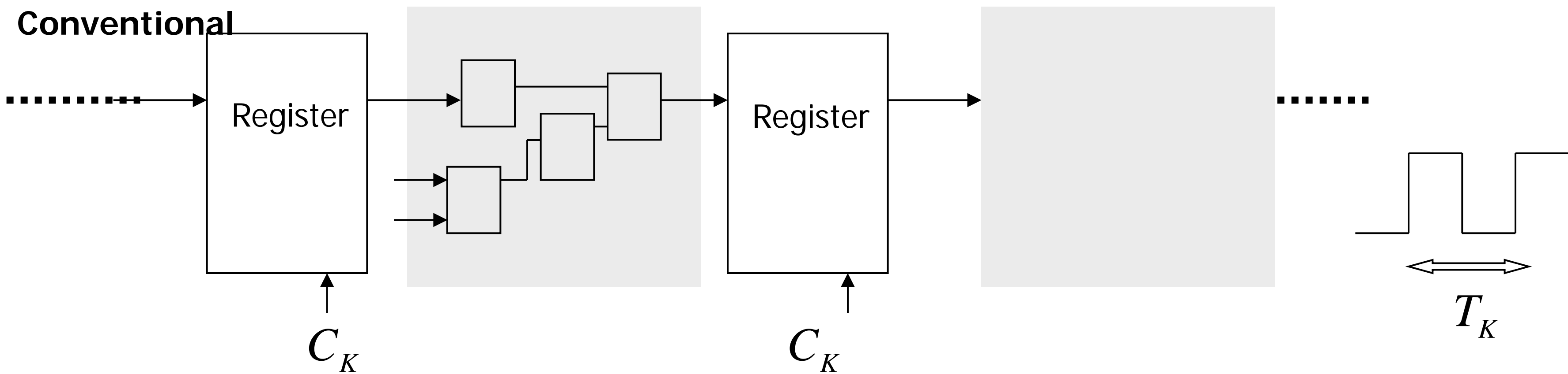
Conventional

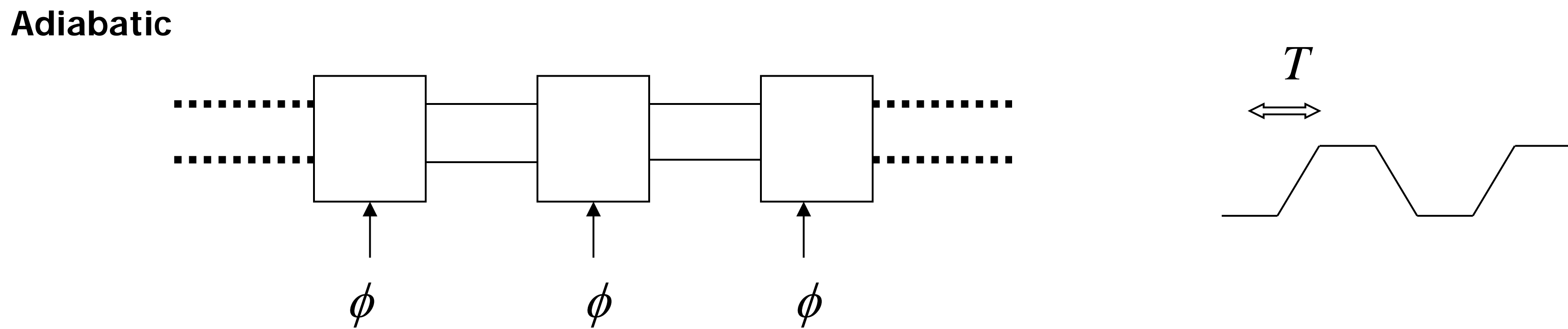
$$E = \alpha \cdot \frac{1}{2} C_L V_{DD}^{2} + \frac{\mu_n C_n}{L^2} V_{th}^{2} e^{-\frac{V_T}{nV_{th}}} V_{DD} T_K \qquad C_n = WLC'_{OX}$$

activity factor betwwen 0.01 and 1

Adiabatic

$$E = \frac{L^2}{C_n} \frac{C_L^{2}}{\mu_n} \frac{V_{DD}^{2}}{\left(V_{DD} - 2V_T\right)} \frac{1}{T} + \frac{\mu_n C_n}{L^2} V_{th}^{2} e^{-\frac{V_T}{nV_{th}}} V_{DD} T$$





$$E_{opt} = \frac{L^2}{C_n}\frac{1}{\mu}\frac{{C_L}^2}{T}\cdot 8V_T$$

$$Topt = \infty \ \ !!!$$

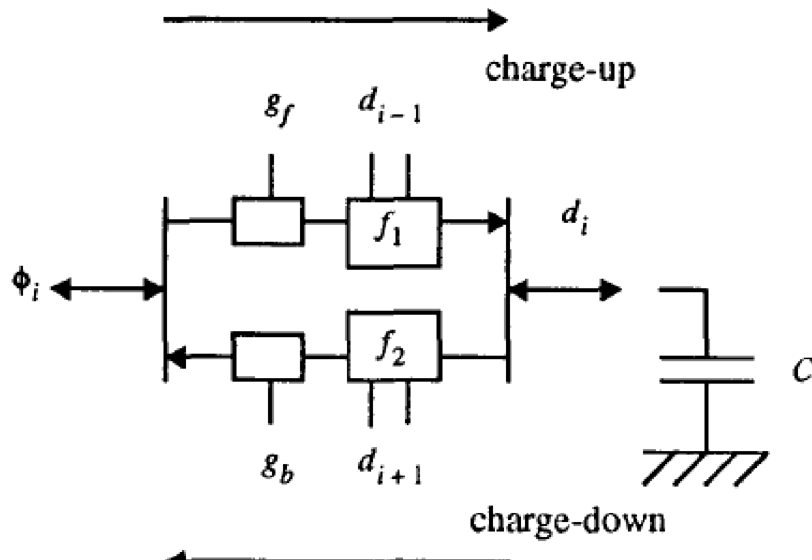
Effect of V_T

Without leakage

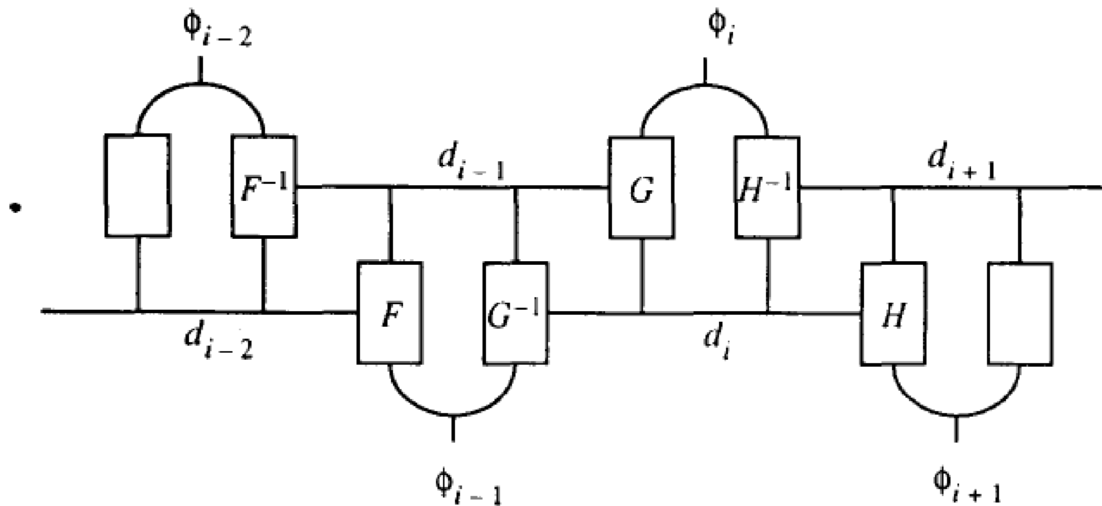
T optimum and E optimum

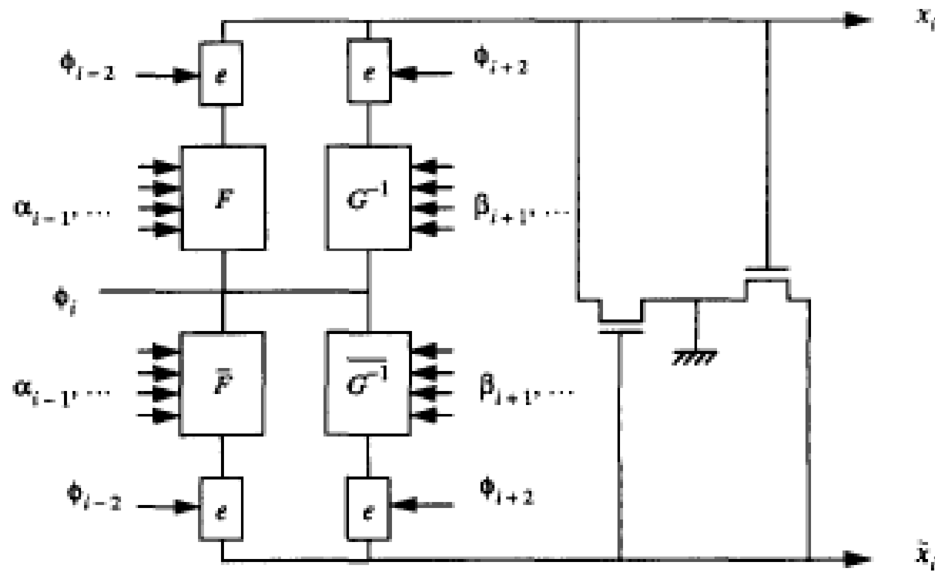
With leakage

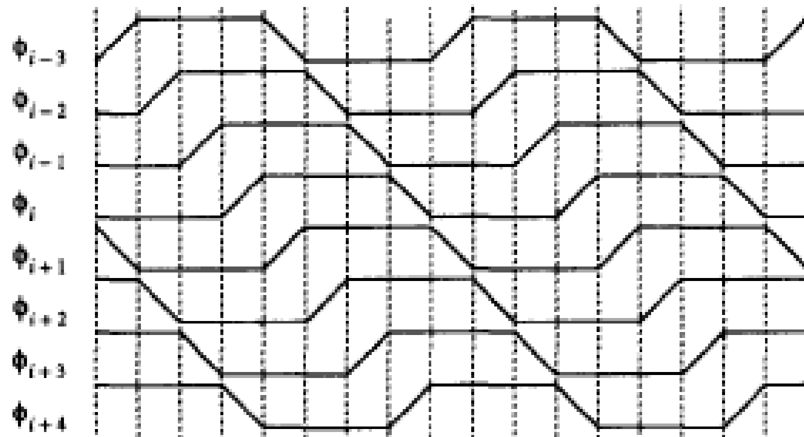
From adiabatic logic to reversible logic



It is necessary to identify inputs from outputs, that is not possible with conventional logic but with reversible gates



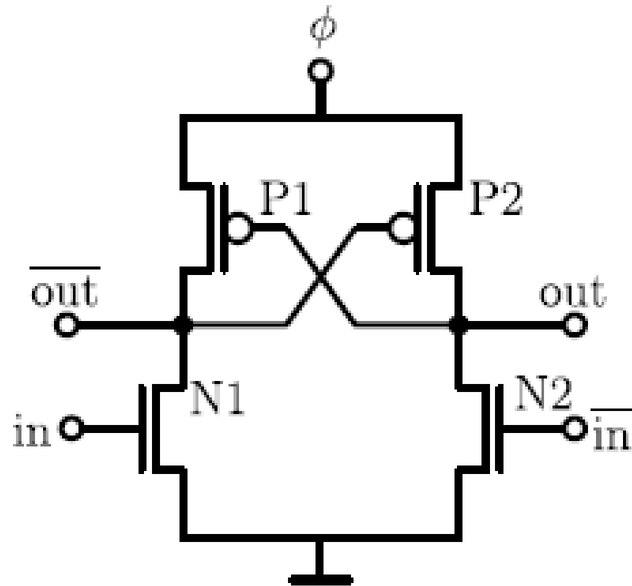


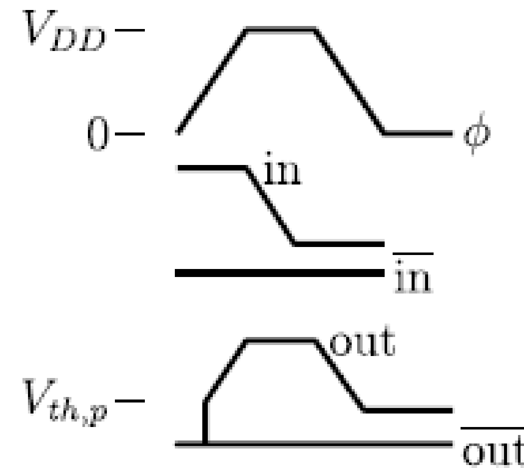


The fully adiabatic pipeline

Fully adiabatic logic is complex but partially adiabatic logic is a good trade-off

The quasi-adiabatic solution





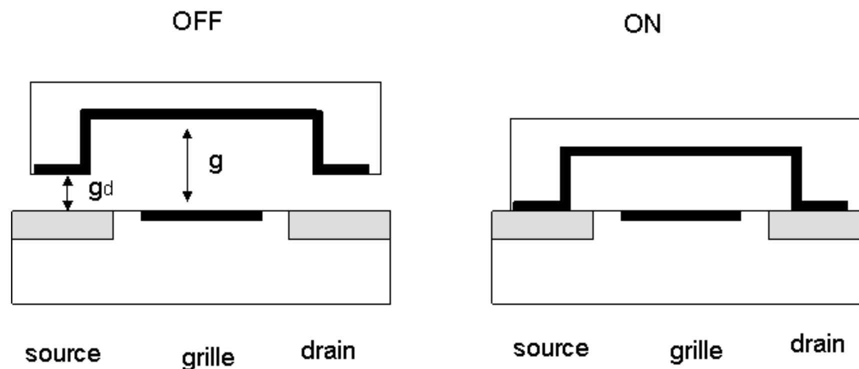
Dissipated energy is not $RC/T \cdot CV^2$

Dissipated energy is $RC/T \cdot CV^2 + C \cdot Vt^2$

Nanorelays for adiabatic logic

The threshold voltage is a limitation with CMOS technology and the subtreshold current a drawback

$$F = \frac{\varepsilon_0 \cdot S \cdot V^2}{2(g - g_d)^2}$$



$$R = 2\frac{4\rho\lambda}{3A} \qquad A = \frac{F}{H\xi}$$

$$V_{PI} = \sqrt{\frac{8kg^3}{27\varepsilon_0 WL}}$$

Leakage is zero

A voltage VPI Is necessary for contact

S electrostatic actuation surface

ρ resistivity of the metal

λ mean free path in metal

H hardness of metal

F electrostatic force

K effective spring constant of the beam

Impact of Scaling on the Performance and Reliability
Degradation of Metal-Contacts in NEMS Devices
Hamed F. Dadgour *, Muhammad M. Hussain **, Alan Cassell †, Navab Singh †† and Kaustav Banerjee *

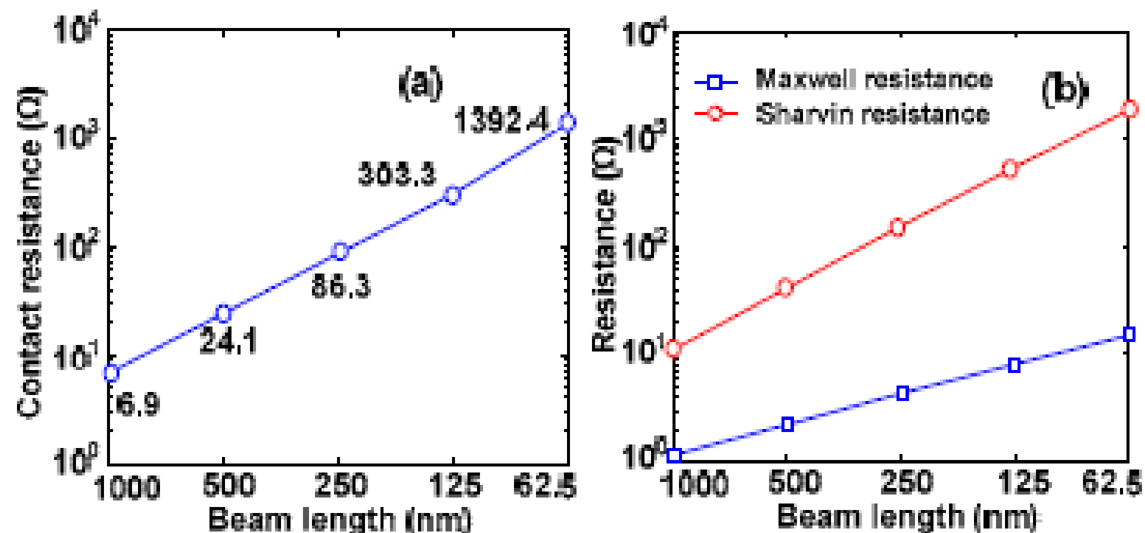
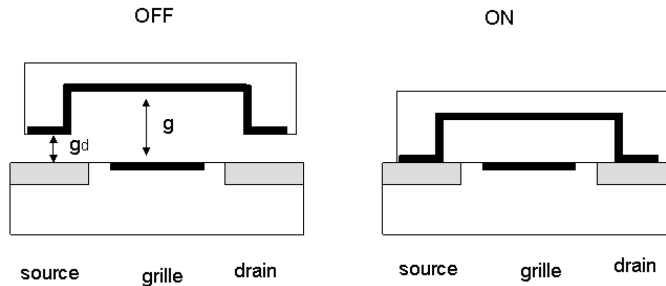


Fig. 15. The impact of scaling on contact resistance: (a) the total contact resistance and (b) contributions of Sharvin and Maxwell resistances to the total resistance.

with adiabatic logic



$$F = \frac{\varepsilon_0 \cdot S \cdot V^2}{2(g - g_d)^2}$$

$$R = 2\frac{4\rho\lambda}{3A}$$

$$A = \frac{F}{H\xi}$$

$$E = \frac{32}{3}\frac{\rho\lambda H\xi}{\varepsilon_0 S}(g - g_d)^2 \frac{C_L^2}{T}$$

If we use this resistance model, energy does not depend on supply voltage !!

Comparison MOS and nanorelays in adiabatic mode

$$E_{nems} = \frac{32}{3}\frac{\rho\lambda H\xi}{C_n}(g-g_d)\frac{C_L{}^2}{T}$$

$$E_{silicium} = \frac{18}{C_n}\frac{L^2}{\mu_n}\frac{C_L{}^2}{T}V_T$$

$$\eta = \frac{E_{nems}}{E_{cmos}} = \frac{10}{18}\frac{\rho\lambda H\xi}{L^2 V_T}(g-g_d)$$

$L = 2\cdot 10^{-8}$

$\mu = 2\cdot 10^{-2}$

$V_T = 0.1$

$\rho = 5\cdot 10^{-8}$

$\lambda = 3\cdot 10^{-8}$

$H = 10^{9}$

$\xi = 0.3$

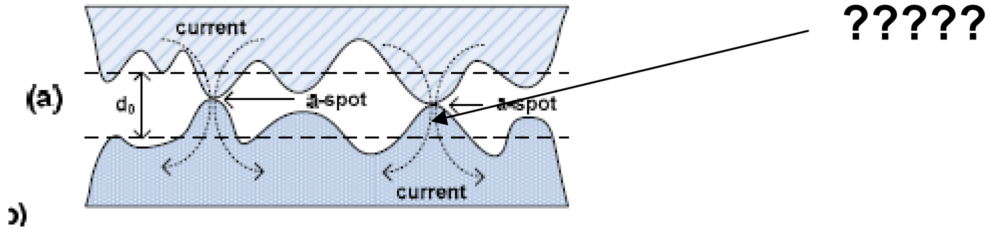
$g - g_d = 10^{-8}$

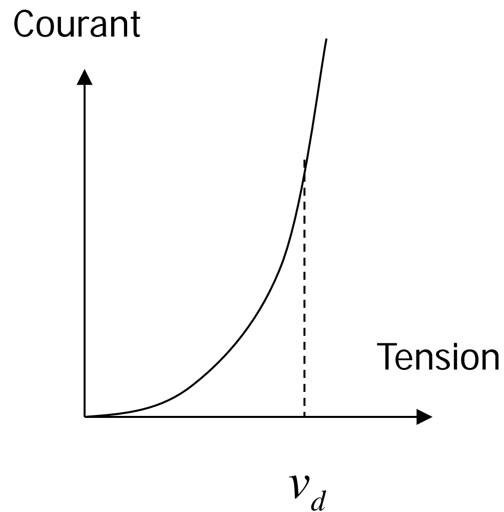
$$\eta = 1.2$$

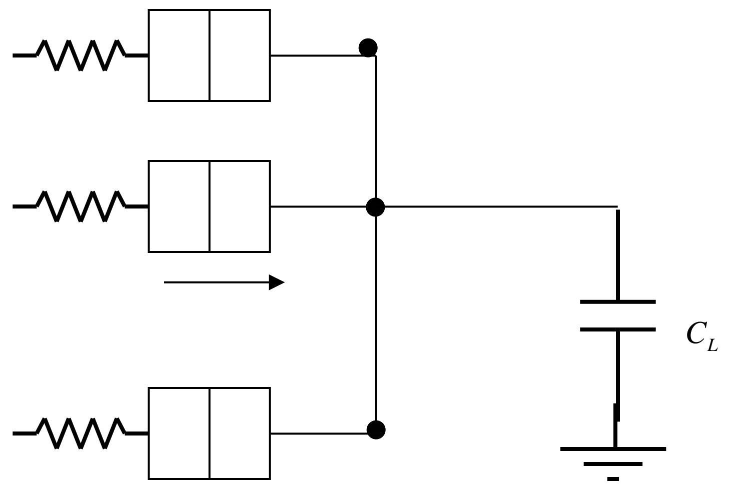
Energies are not so different but models have to be confirmed

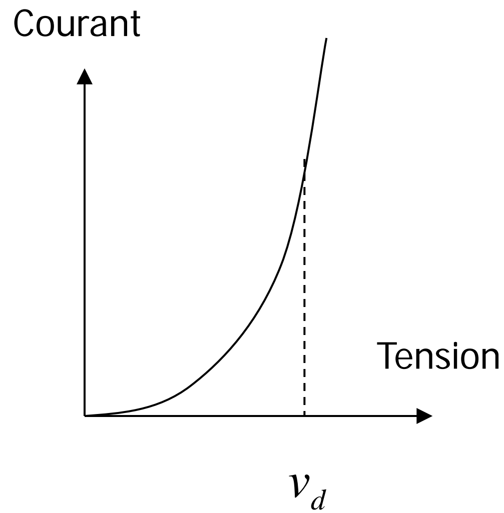
Zero leakage is the main advantage of nanorelays

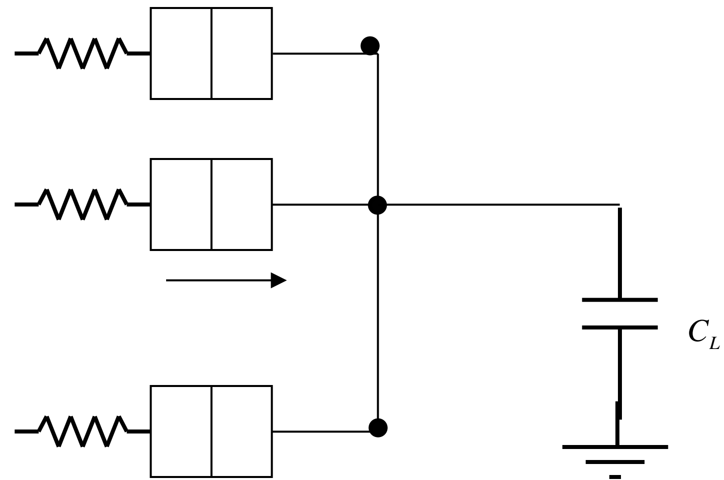
What kind of contact at nanoscale ?











$$E = \frac{32}{3}\frac{\rho\lambda H\xi}{\varepsilon_0 S}\left(g - g_d\right)^2 \frac{C_L{}^2}{T} + C_L V_{DD} v_d$$

Non adiabatic dissipation

Trade-off reliability-energy efficiency

Integrated Circuit Design with NEM Relays

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The best-known contact material for minimum contact resistance is gold (Au), which has a hardness of 0.2-0.7GPa, a resistivity of 23nΩ·m, and an electron mean free path of 36 nm. **For the 90 nm equivalent** devices used in our circuit study, the total contactresistance of a gold-based elastic-contact relay design is estimated to be on the order of **100 Ω even at a low *V*gb of 0.3 V**.

Unfortunately, gold may not be suitable for fabrication of nanoscalefeatures with fine pitch, and other more suitable materials are typically harder and hence have higher contact resistance. For example, if the physical contacts are instead formed with tungsten(W), which has a hardness of 1.1 GPa, resistivity of 55 nΩ·m, and electron mean free path of 33 nm, the estimated total contact resistance for an elastic contact at a *V*gb of **0.3 V is ~1 kΩ**. In our circuit study we will present results for both the best-case(gold) and worst-case (tungsten) contact materials, including thereduction in contact resistance as a function of supply voltage.

Conclusions

- Energy efficiency is the main nanoelecronic driver…
- Many improvements at circuit level
- New switches (Tunnel FET and NEMS) have to be confirmed for future ultra low power electronics but FDSOI and FinFETs are today solutions
- Adiabatic logic in association with new switches has to be investigated

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February 2010 vol 98 Number 2

Circuit technology for ultra low power