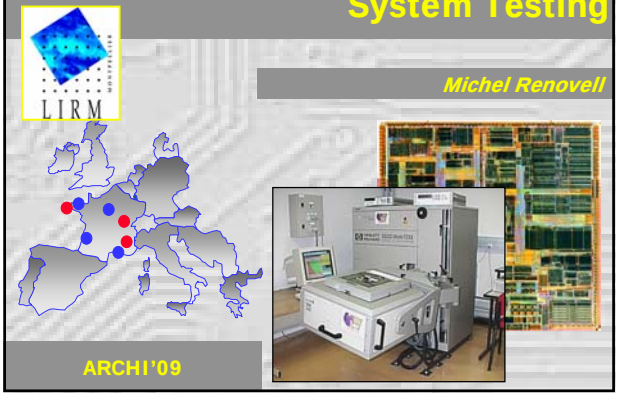
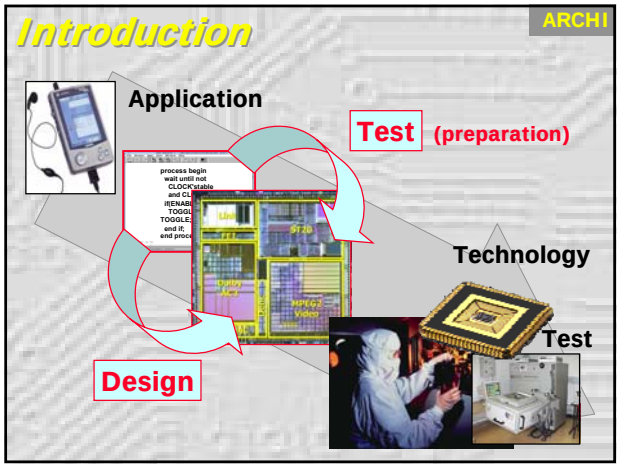
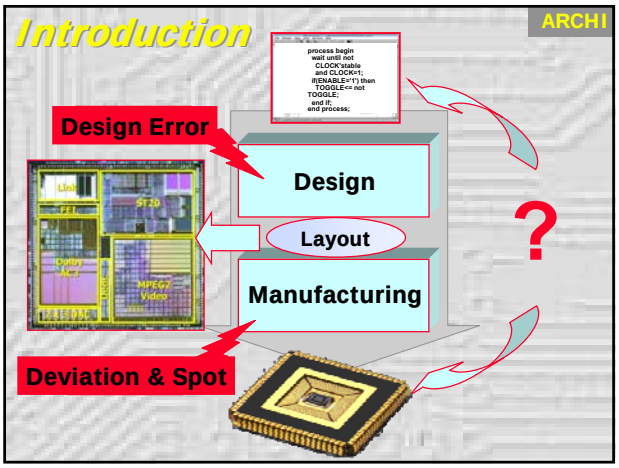
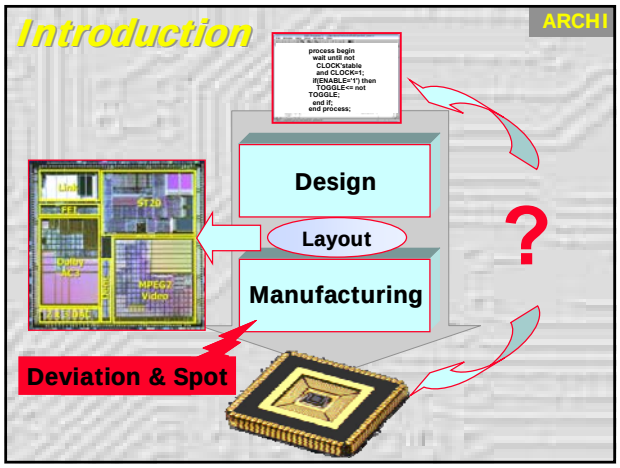
Fundamentals of Digital & Analog System Testing



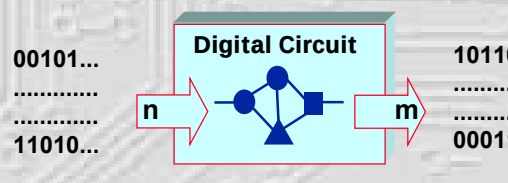






Introduction

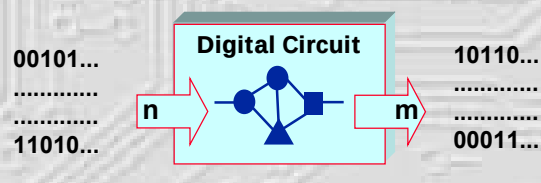
ARCHI



- Boolean Testing
- Test Patterns
- Go/NoGo

Introduction

ARCHI

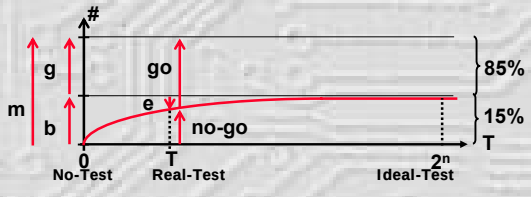


- Exhaustive Testing
- 2^{64} patterns
- 10^{19}/100MHz = 10^{11}s
- => 5850 years

- Realistic Test
- 10s / 100MHz
- 10^{9}
- 1 / 10^{10}

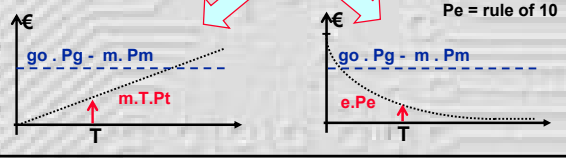
Introduction

ARCHI



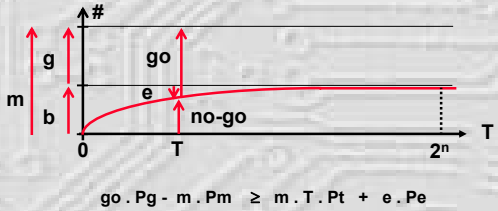
go . Pg - m . Pm > Margin

Y = 75%
e = 500 ppm
Pe = rule of 10

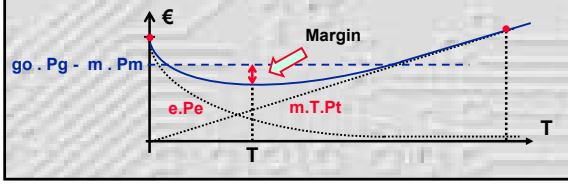


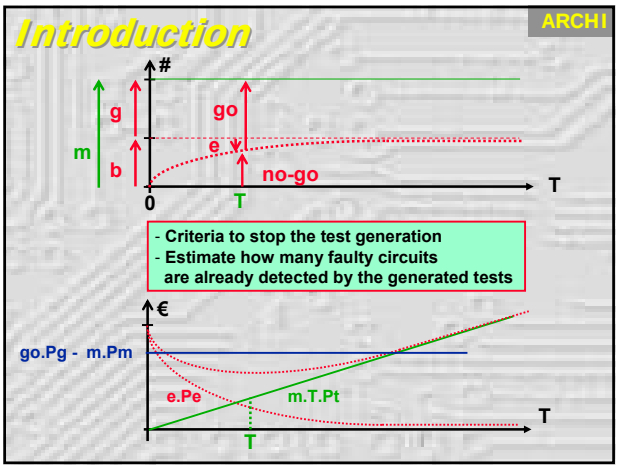
Introduction

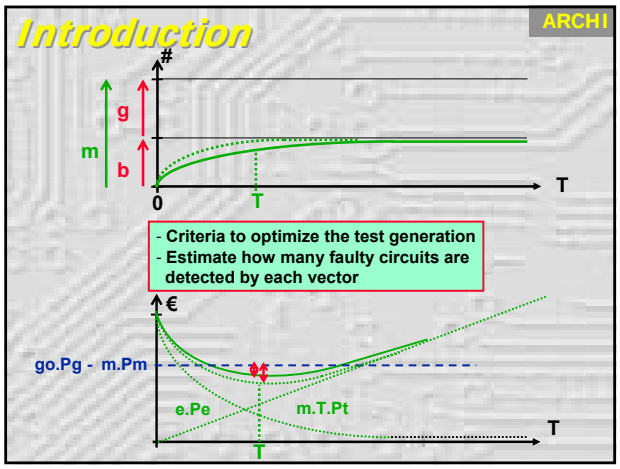
ARCHI

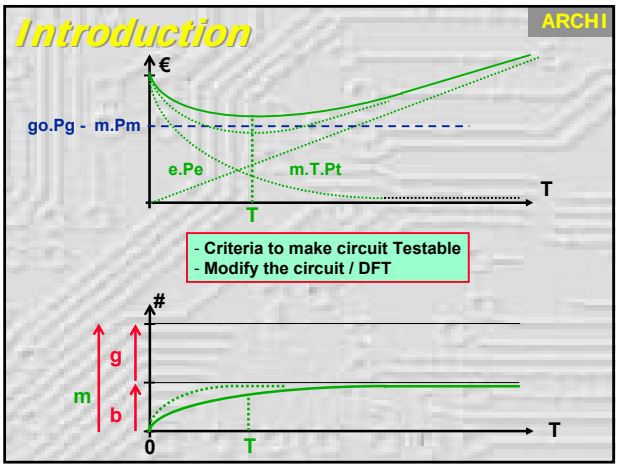


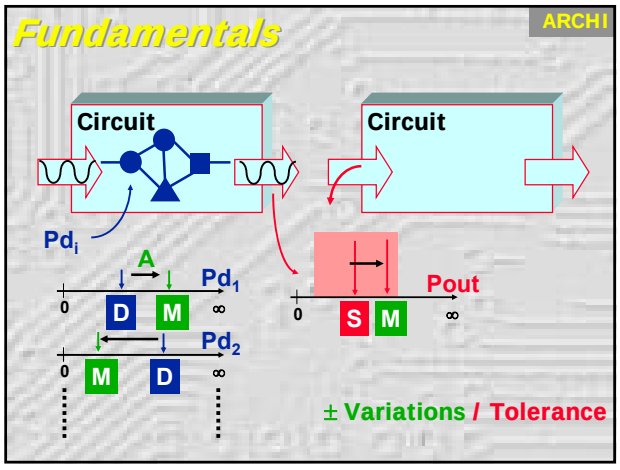
go . Pg - m . Pm ≥ m . T . Pt + e . Pe

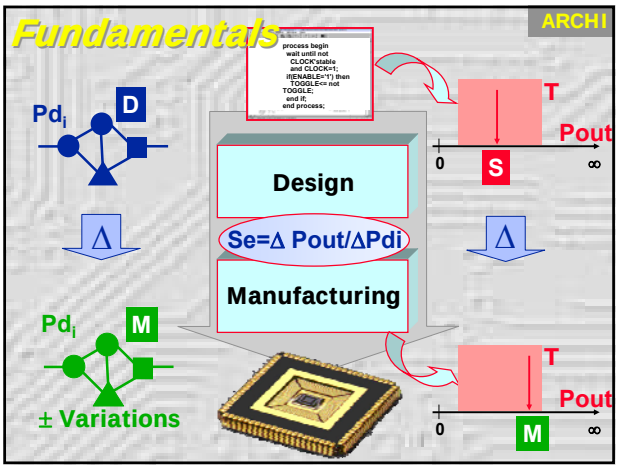


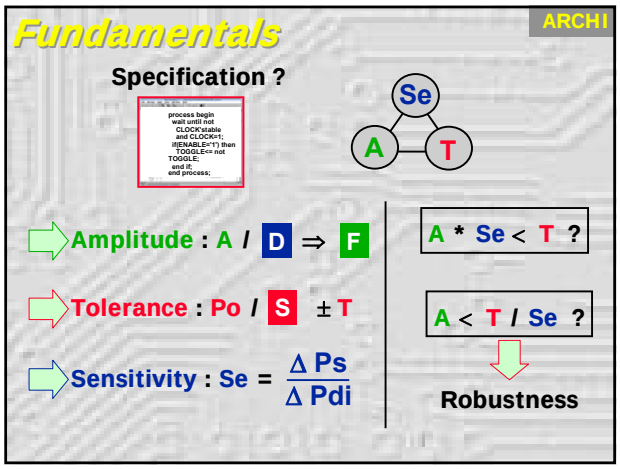

Introduction
ARCHI
#
g
m
b
go
e
no-go
0
T
T
- Criteria to stop the test generation
- Estimate how many faulty circuits
are already detected by the generated tests
€
go.Pg - m.Pm
e.Pe
m.T.Pt
T
T

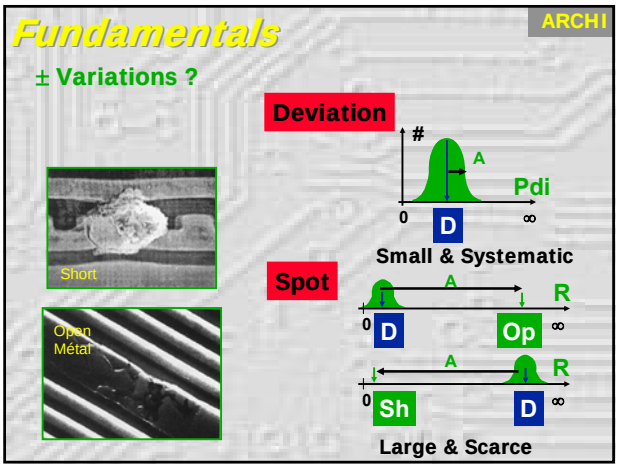

Introduction
ARCHI
#
g
m
b
0
T
T
- Criteria to optimize the test generation
- Estimate how many faulty circuits are
detected by each vector
€
go.Pg - m.Pm
e.Pe
m.T.Pt
T
T

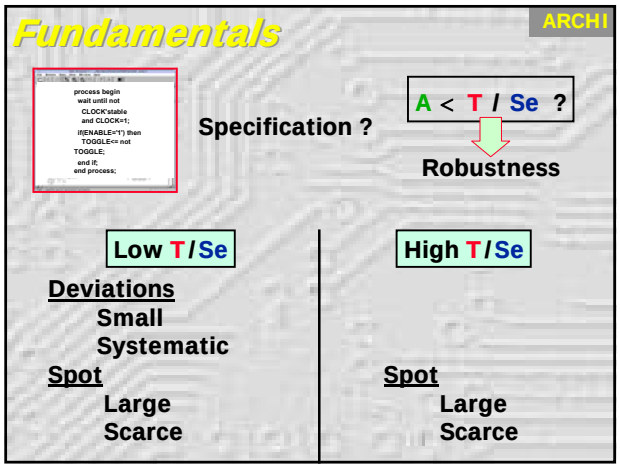

Introduction
ARCHI
€
go.Pg - m.Pm
e.Pe
m.T.Pt
T
T
- Criteria to make circuit Testable
- Modify the circuit / DFT
#
g
m
b
0
T
T

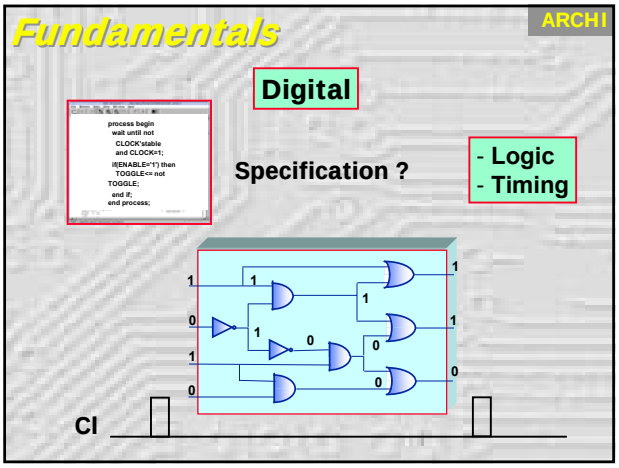

Fundamentals
ARCHI
Circuit
Circuit
Pdi
A
Pd1
0
D
M
∞
Pd2
0
M
D
∞
Pout
0
S
M
∞
± Variations / Tolerance

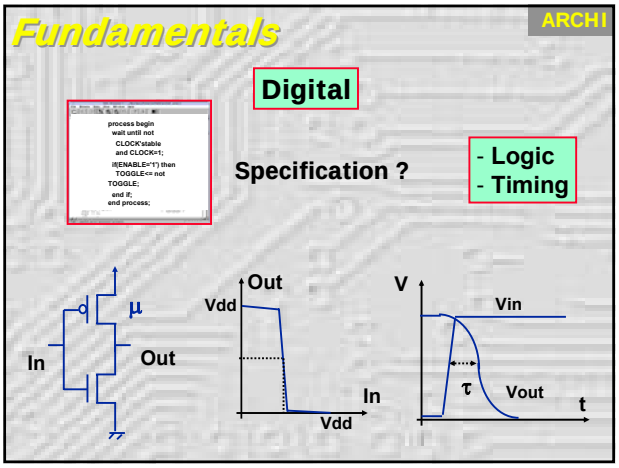

Fundamentals
ARCHI
Pdi
D
Design
Se=Δ Pout/ΔPdi
Manufacturing
Pdi
M
± Variations
T
Pout
0
S
∞
T
Pout
0
M
∞

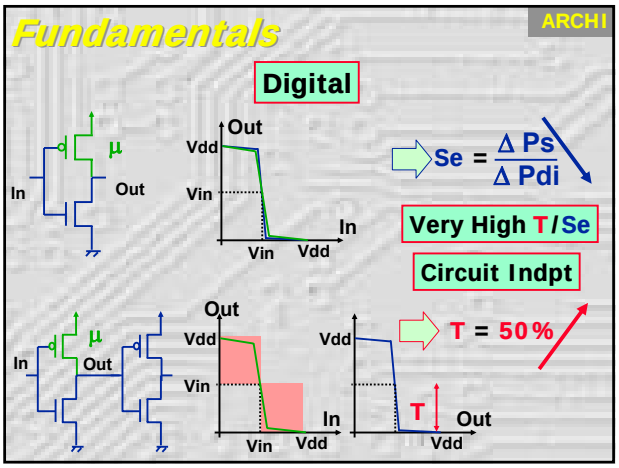

Fundamentals
ARCHI
Specification ?
Se
A
T
Amplitude : A / D ⇒ F
Tolerance : Po / S ± T
Sensitivity : Se = Δ Ps / Δ Pdi
A * Se < T ?
A < T / Se ?
Robustness

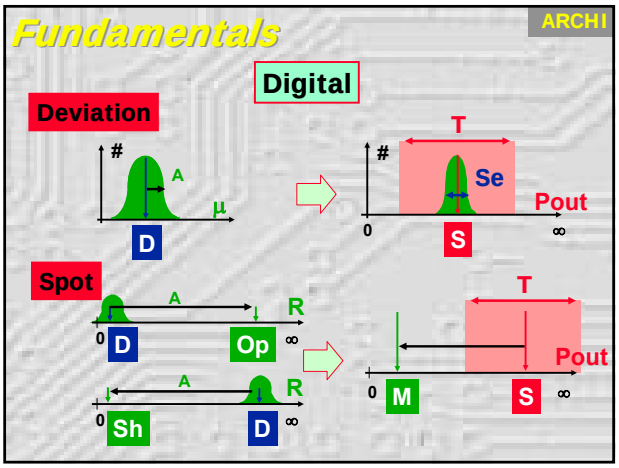

Fundamentals
ARCHI
± Variations ?
Short
Open
Métal
Deviation
#
A
Pdi
0
D
∞
Small & Systematic
Spot
A
R
0
D
Op
∞
A
R
0
Sh
D
∞
Large & Scarce

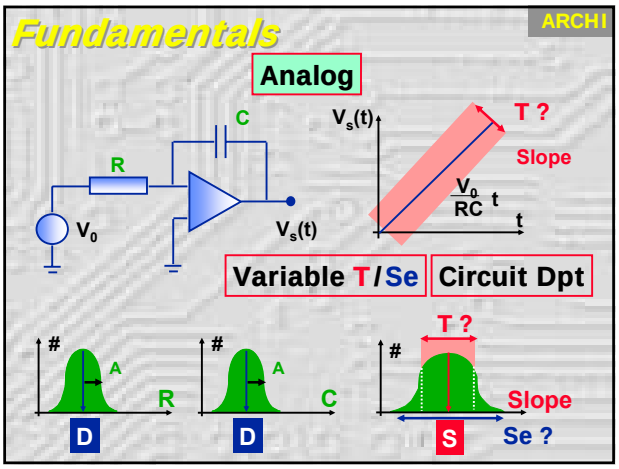

Fundamentals
ARCHI
Specification ?
A < T / Se ?
Robustness
Low T/Se
Deviations
Small
Systematic
Spot
Large
Scarce
High T/Se
Spot
Large
Scarce

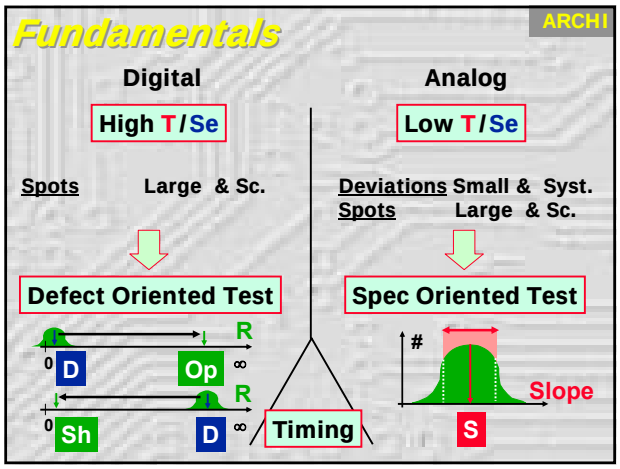

Fundamentals
ARCHI
Digital
Specification ?
- Logic
- Timing
Cl

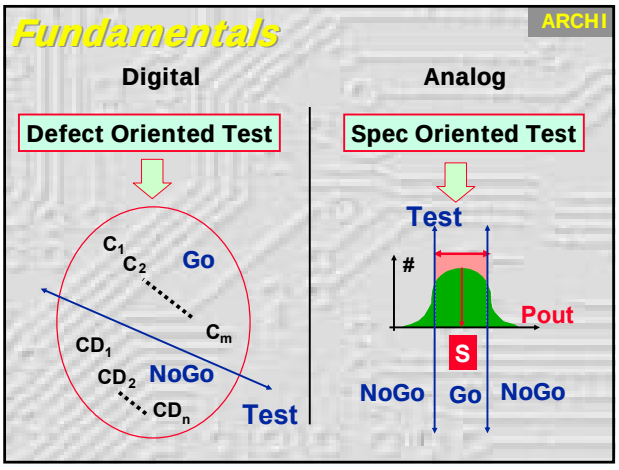

Fundamentals
ARCHI
Digital
Specification ?
- Logic
- Timing
In
Out
Vdd
V
Vin
Vout
t

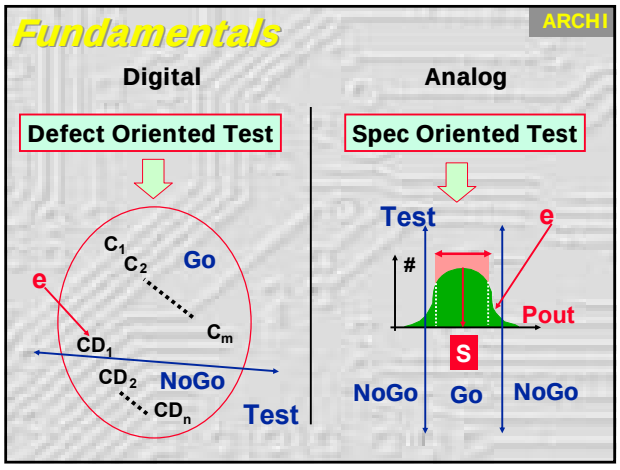

Fundamentals
ARCHI
Digital
In
Out
Vdd
Vin
Se = Δ Ps / Δ Pdi
Very High T/Se
Circuit Indpt
T = 50 %
T

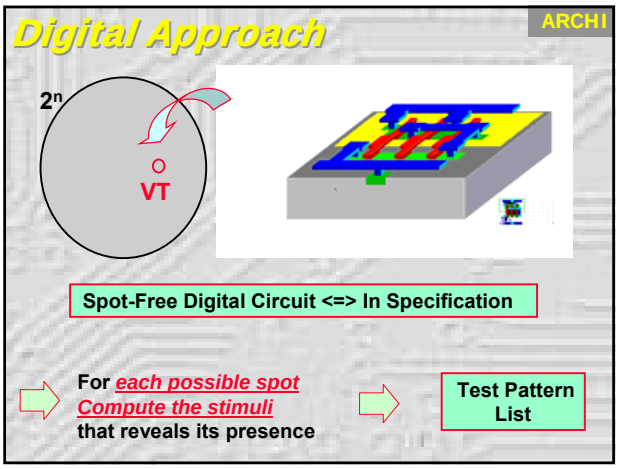

Fundamentals
ARCHI
Digital
Deviation
Spot
D
S
Op
Sh
M
Se
Pout
T

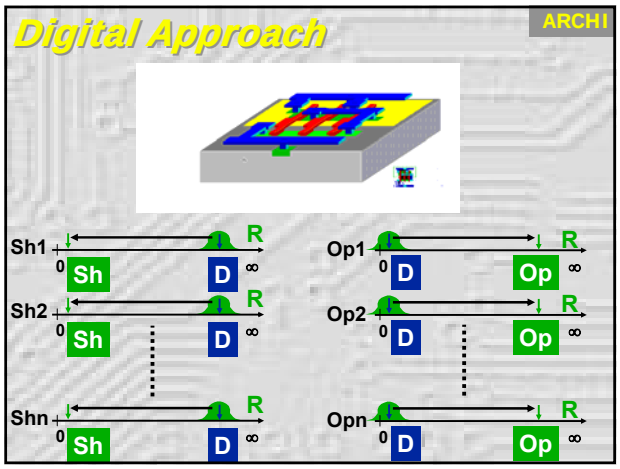

Fundamentals
ARCHI
Analog
C
R
V0
Vs(t)
Vs(t)
T ?
Slope
V0/RC t
t
Variable T/Se
Circuit Dpt
#
A
R
D
#
A
C
D
T ?
#
Slope
S
Se ?

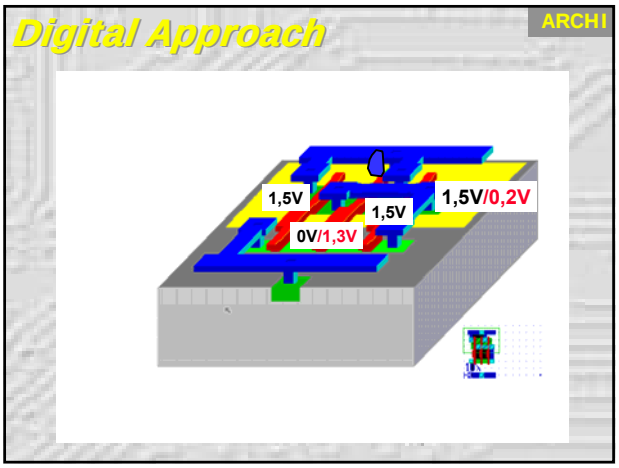

Fundamentals
ARCHI
Digital
Analog
High T/Se
Low T/Se
Spots
Large & Sc.
Deviations
Spots
Small & Syst.
Large & Sc.
Defect Oriented Test
Spec Oriented Test
R
0
D
Op
∞
R
0
Sh
D
∞
Timing
#
Slope
S

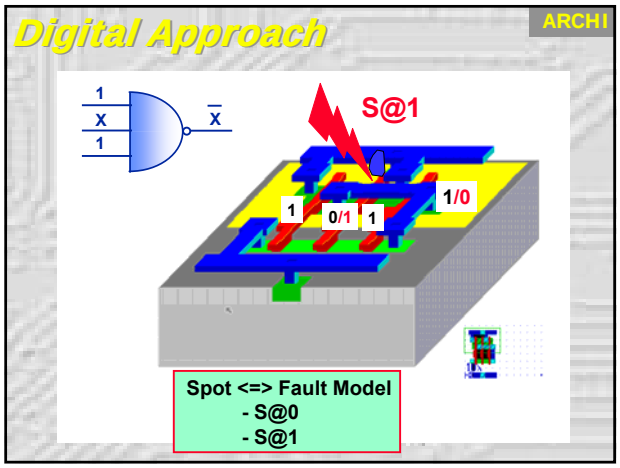

Fundamentals
ARCHI
Digital
Analog
Defect Oriented Test
Spec Oriented Test
C1
C2
Go
Cm
CD1
CD2
NoGo
CDn
Test
Test
#
Pout
S
NoGo
Go
NoGo


Fundamentals
ARCHI
Digital
Analog
Defect Oriented Test
Spec Oriented Test
e
C1
C2
Go
Cm
CD1
CD2
NoGo
CDn
Test
Test
e
#
Pout
S
NoGo
Go
NoGo


Digital Approach
ARCHI
2n
VT
Spot-Free Digital Circuit <=> In Specification
For each possible spot
Compute the stimuli
that reveals its presence
Test Pattern
List

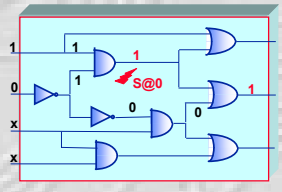

Digital Approach
ARCHI
Sh1
Sh2
Shn
Op1
Op2
Opn
Sh
Op
D
R
0
∞


Digital Approach
ARCHI
1,5V
1,5V
0V/1,3V
1,5V/0,2V


Digital Approach
ARCHI
1
X
1
X
S@1
1
0/1
1
1/0
Spot <=> Fault Model
- S@0
- S@1

Digital Approach

ARCHI



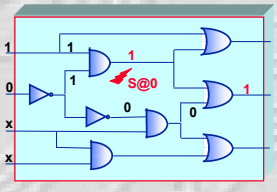
Cost

- 10^6 gates
- 10^6 nodes
- 10^6 S@0
- 10^6 S@1
- 2.10^6 vectors
- 100Mhz

Physical Structure <=> Logical Structure
- Each Logic node S@0
- Each Logic node S@1
- TPG

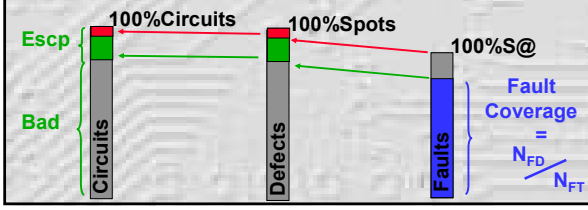
Digital Approach

ARCHI



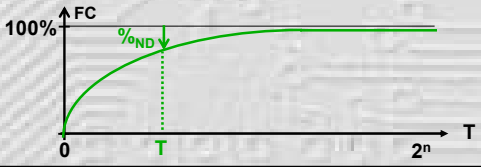
Cost

- 10^6 S@0
- 10^6 S@1
- 2.10^6 vectors



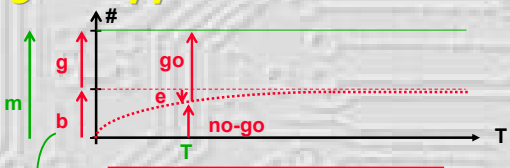
Digital Approach

ARCHI

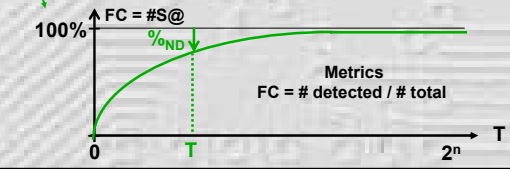


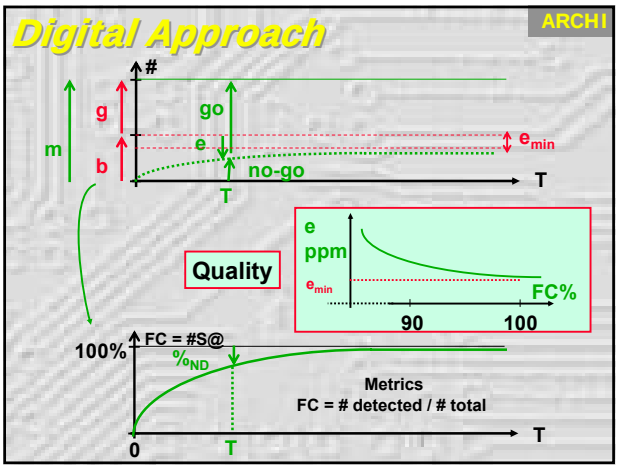
Digital Approach

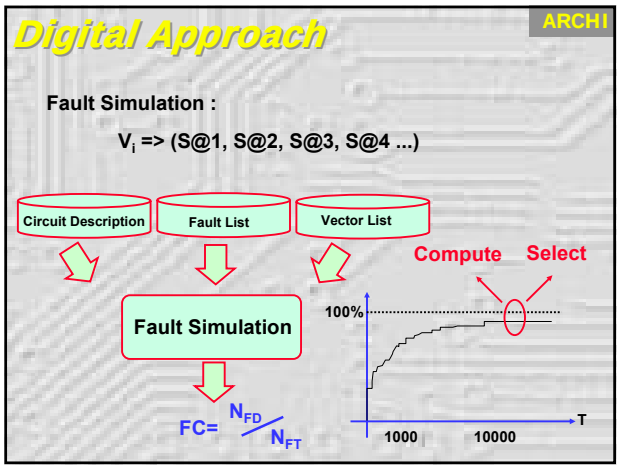
ARCHI

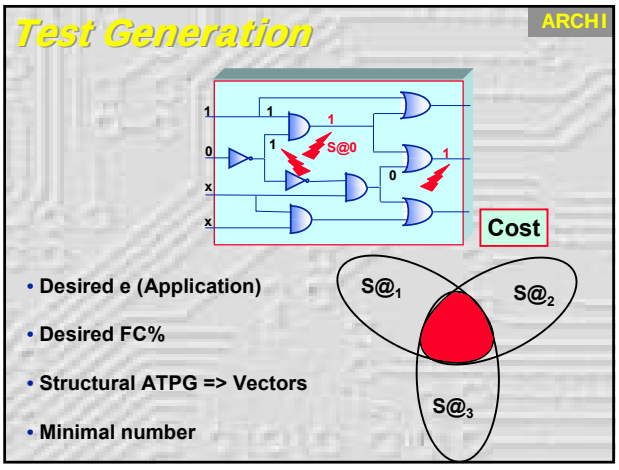


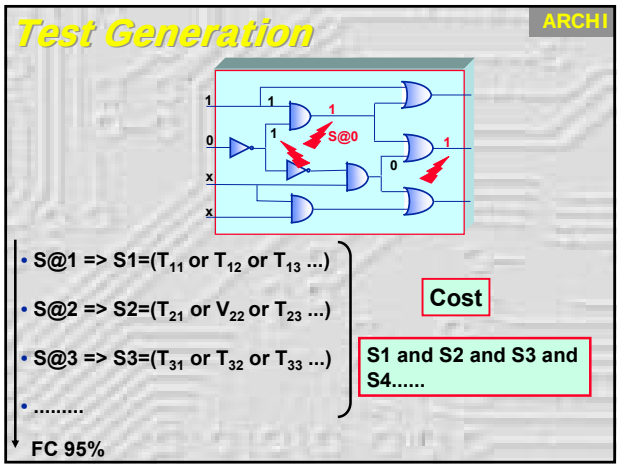
- Criteria to optimize the test generation
- Estimate how many faulty circuits are detected by each vector




Digital Approach
ARCHI
#
g
go
m
e
b
no-go
T
e_{min}
T
e
ppm
e_{min}
FC%
90
100
Quality
100%
FC = #S@
$\%_{ND}$
Metrics
FC = # detected / # total
0
T
T

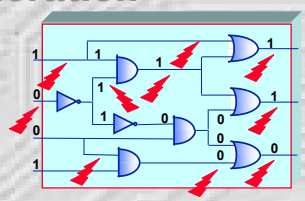

Digital Approach
ARCHI
Fault Simulation :
V_i => (S@1, S@2, S@3, S@4 ...)
Circuit Description
Fault List
Vector List
Compute
Select
Fault Simulation
100%
FC= N_{FD} / N_{FT}
1000
10000
T


Test Generation
ARCHI
S@0
Cost
• Desired e (Application)
• Desired FC%
• Structural ATPG => Vectors
• Minimal number
S@1
S@2
S@3


Test Generation
ARCHI
S@0
• S@1 => S1=(T_{11} or T_{12} or T_{13} ...)
• S@2 => S2=(T_{21} or V_{22} or T_{23} ...)
• S@3 => S3=(T_{31} or T_{32} or T_{33} ...)
• .....
FC 95%
Cost
S1 and S2 and S3 and S4.....

Test Generation

ARCHI



Cost

- ATPG :

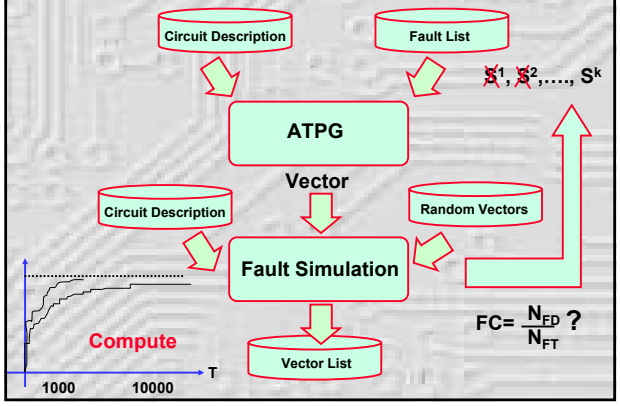
  S@1 => T_{11} (np)

- Fault Simulation :

  V_{ij} => (S@1, S@2, S@3, S@4 ...) (ok)

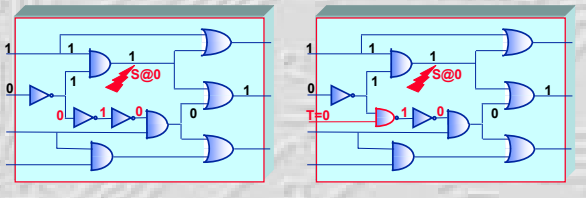
Test Generation

ARCHI



DFT

ARCHI

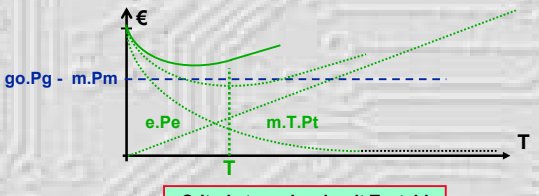


- ATPG / Backtrack
- FC < Desired FC
- Modify the Structure

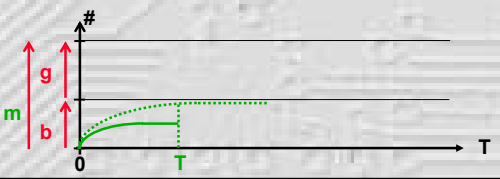
Design For Test

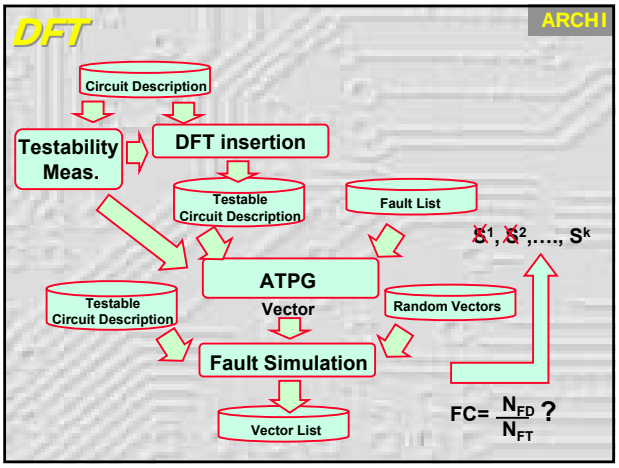
DFT

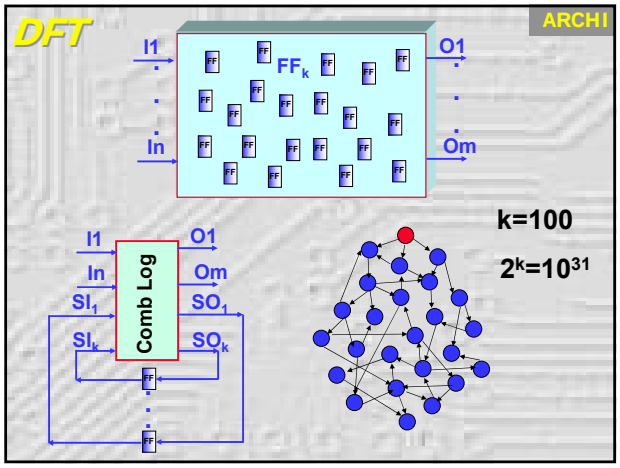
ARCHI

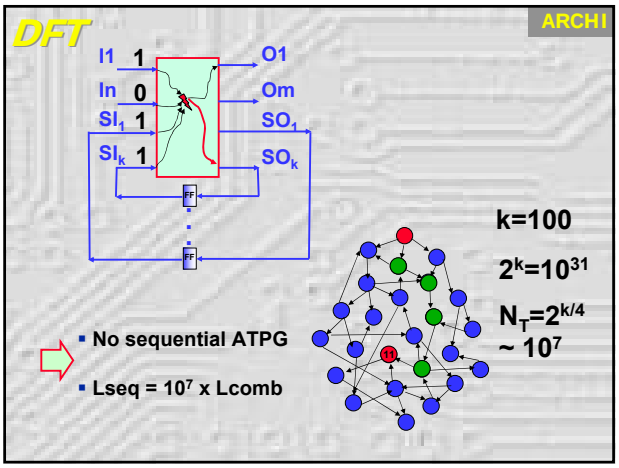


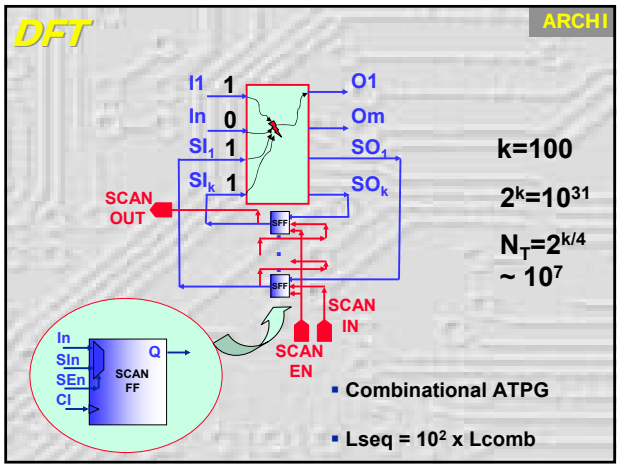
- Criteria to make circuit Testable
- Modify the circuit / DFT

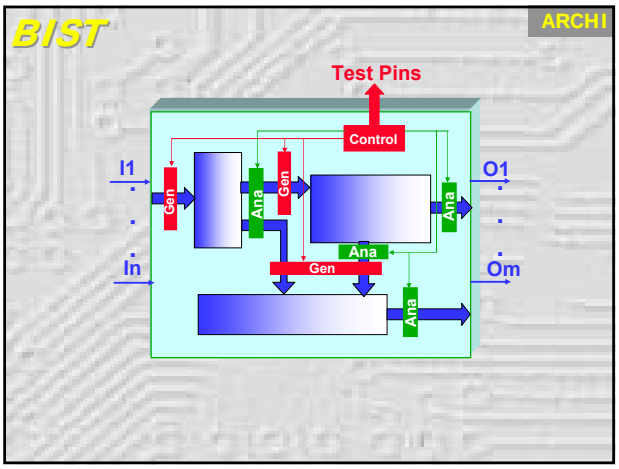


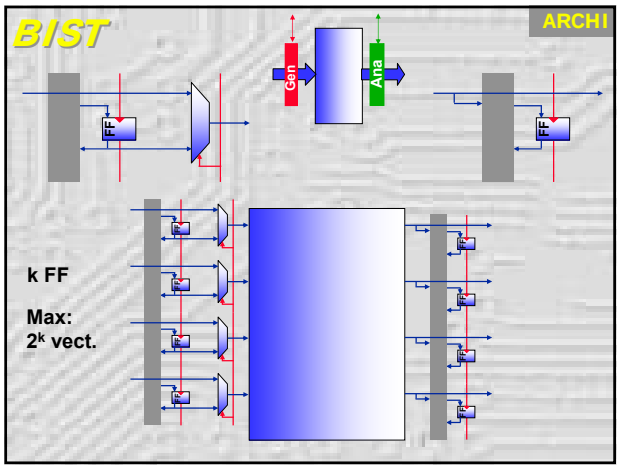

DFT
ARCHI
Circuit Description
Testability Meas.
DFT insertion
Testable Circuit Description
Fault List
S1, S2,…., Sk
ATPG
Vector
Testable Circuit Description
Random Vectors
Fault Simulation
Vector List
FC= NFD / NFT ?

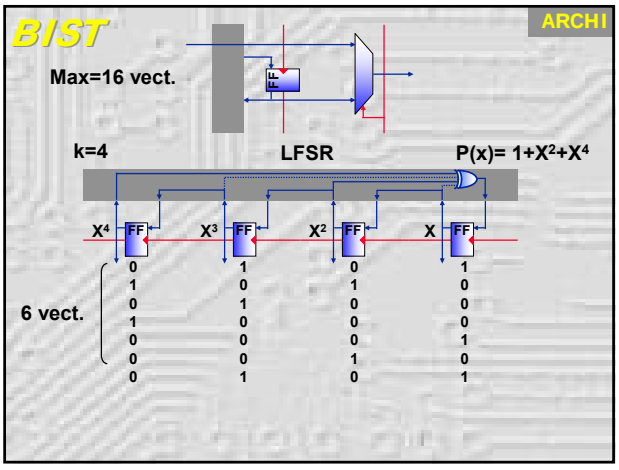

DFT
ARCHI
I1
In
FFk
O1
Om
Comb Log
SI1
SIk
SO1
SOk
k=100
2k=1031

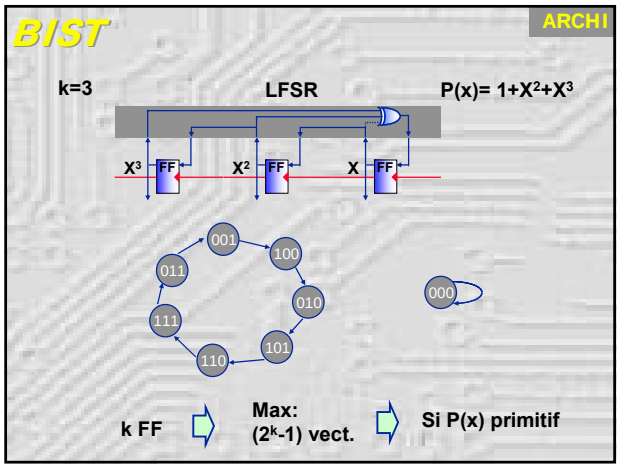

DFT
ARCHI
I1 1
In 0
SI1 1
SIk 1
O1
Om
SO1
SOk
▪ No sequential ATPG
▪ Lseq = 107 x Lcomb
k=100
2k=1031
NT=2k/4
~ 107

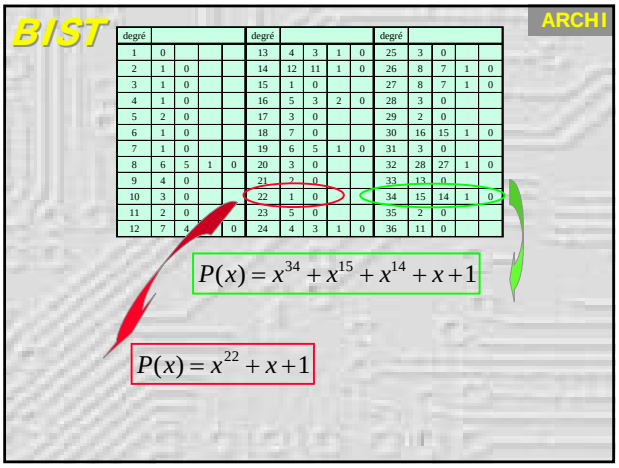

DFT
ARCHI
I1 1
In 0
SI1 1
SIk 1
O1
Om
SO1
SOk
SCAN OUT
SCAN IN
SCAN EN
In
SIn
SEn
CI
Q
SCAN FF
▪ Combinational ATPG
▪ Lseq = 102 x Lcomb
k=100
2k=1031
NT=2k/4
~ 107

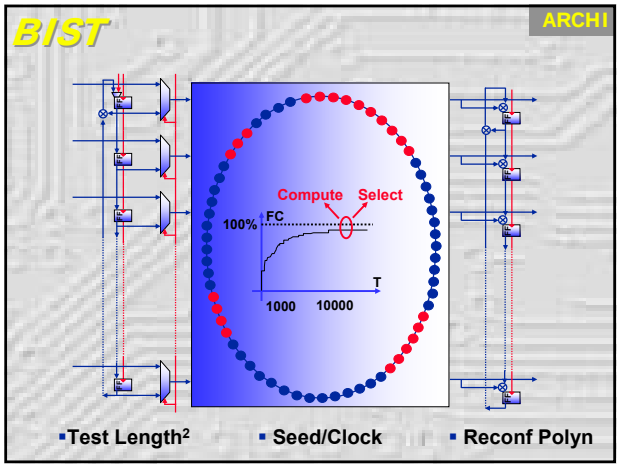

BIST
ARCHI
Test Pins
Control
I1
In
O1
Om
Gen
Ana
Gen
Ana
Ana
Gen
Ana

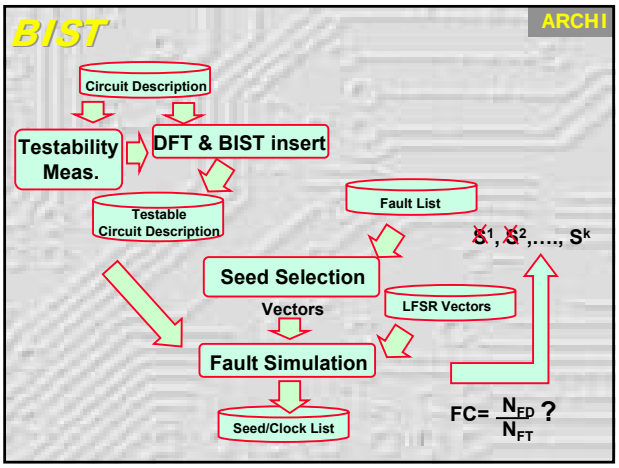

BIST
ARCHI
Gen
Ana
FF
k FF
Max:
2k vect.

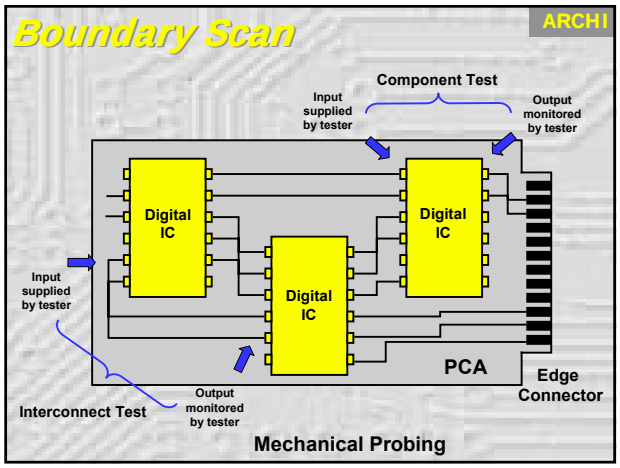

BIST
ARCHI
Max=16 vect.
FF
k=4
LFSR
P(x)= 1+X2+X4
X4
X3
X2
X
FF
6 vect.
0 1 0 1 0 0 0
1 0 1 0 0 0 1
0 1 0 0 0 1 0
1 0 0 0 1 0 1

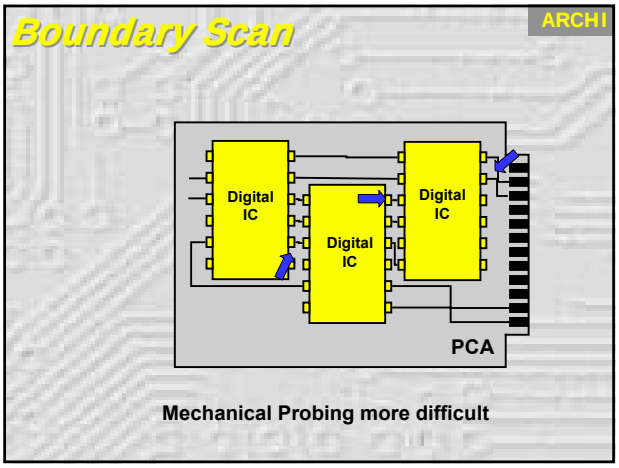

BIST
ARCHI
k=3
LFSR
P(x)= 1+X2+X3
X3
X2
X
FF
001
100
011
010
111
101
110
000
k FF
Max:
(2k-1) vect.
Si P(x) primitif

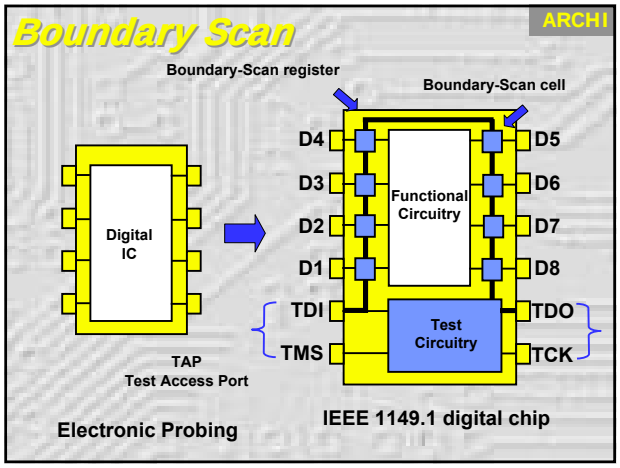

BIST
ARCHI
$P(x) = x^{34} + x^{15} + x^{14} + x + 1$
$P(x) = x^{22} + x + 1$

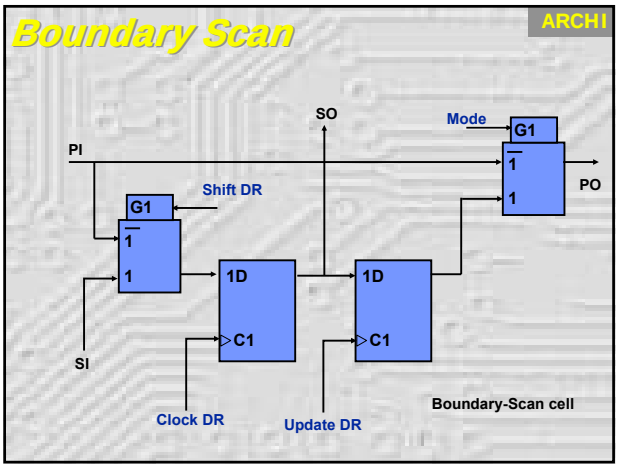

BIST
ARCHI
Compute
Select
100%
FC
T
1000
10000
Test Length²
Seed/Clock
Reconf Polyn

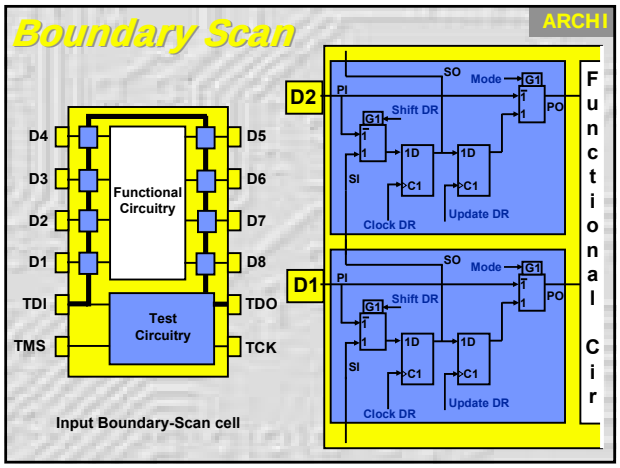

BIST
ARCHI
Circuit Description
Testability Meas.
DFT & BIST insert
Testable Circuit Description
Fault List
$S^1, S^2, \ldots, S^k$
Seed Selection
Vectors
LFSR Vectors
Fault Simulation
Seed/Clock List
FC= $\frac{N_{FD}}{N_{FT}}$?

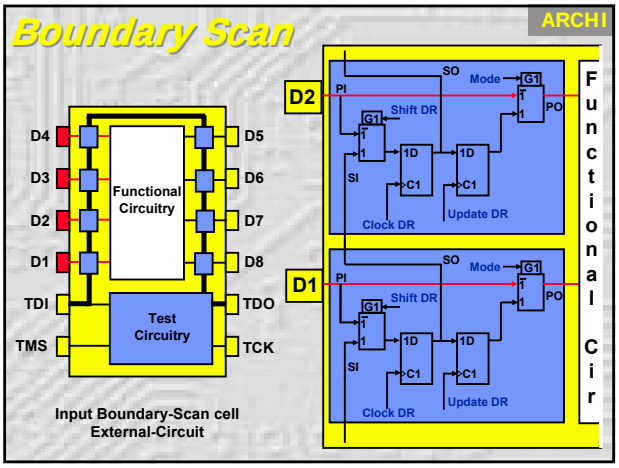

Boundary Scan
ARCHI
Component Test
Input supplied by tester
Output monitored by tester
Digital IC
Digital IC
Digital IC
Input supplied by tester
PCA
Edge Connector
Interconnect Test
Output monitored by tester
Mechanical Probing

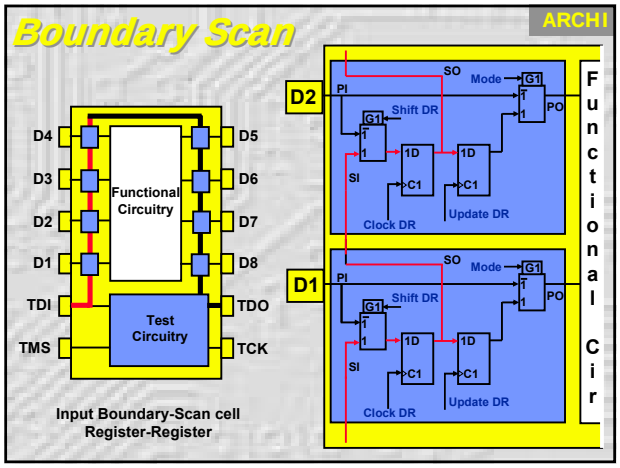

Boundary Scan
ARCHI
Digital IC
Digital IC
Digital IC
PCA
Mechanical Probing more difficult

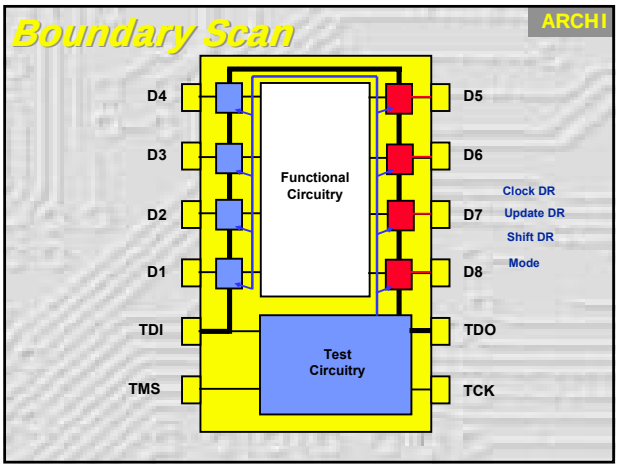

Boundary Scan
ARCHI
Boundary-Scan register
Boundary-Scan cell
Digital IC
D4
D3
D2
D1
TDI
TMS
D5
D6
D7
D8
TDO
TCK
Functional Circuitry
Test Circuitry
TAP
Test Access Port
Electronic Probing
IEEE 1149.1 digital chip

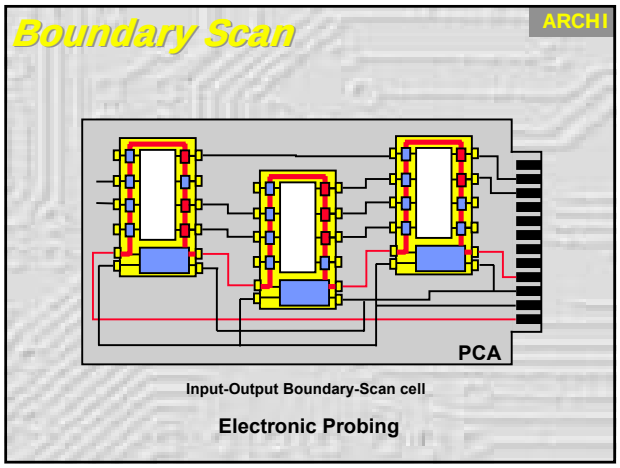

Boundary Scan
ARCHI
PI
SO
Mode
G1
PO
Shift DR
G1
1
1
1D
C1
1D
C1
SI
Clock DR
Update DR
Boundary-Scan cell

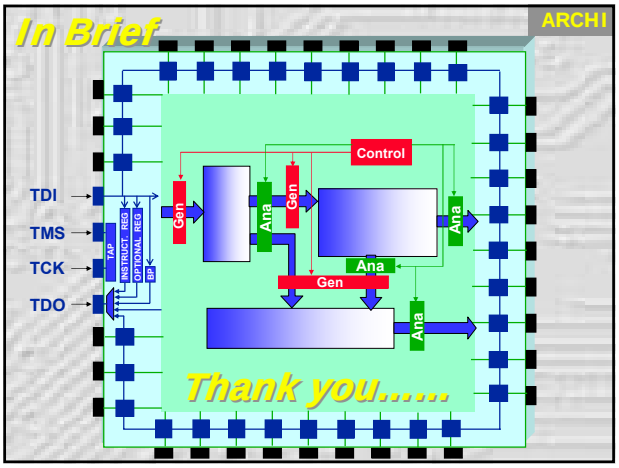

Boundary Scan
ARCHI
D4
D3
D2
D1
TDI
TMS
D5
D6
D7
D8
TDO
TCK
Functional Circuitry
Test Circuitry
Input Boundary-Scan cell
D2
D1
SO
Mode
G1
PI
PO
Shift DR
SI
1D
C1
Clock DR
Update DR
Functional Cir


Boundary Scan
ARCHI
D4
D3
D2
D1
TDI
TMS
D5
D6
D7
D8
TDO
TCK
Functional Circuitry
Test Circuitry
D2
D1
PI
SO
Mode
G1
Shift DR
PO
SI
1D
C1
Clock DR
Update DR
Functional Cir
Input Boundary-Scan cell
External-Circuit


Boundary Scan
ARCHI
D4
D3
D2
D1
TDI
TMS
D5
D6
D7
D8
TDO
TCK
Functional Circuitry
Test Circuitry
D2
D1
PI
SO
Mode
G1
Shift DR
PO
SI
1D
C1
Clock DR
Update DR
Functional Cir
Input Boundary-Scan cell
Register-Register


Boundary Scan
ARCHI
D4
D3
D2
D1
TDI
TMS
D5
D6
D7
D8
TDO
TCK
Functional Circuitry
Test Circuitry
Clock DR
Update DR
Shift DR
Mode


Boundary Scan
ARCHI
PCA
Input-Output Boundary-Scan cell
Electronic Probing


In Brief
ARCHI
Control
TDI
TMS
TCK
TDO
TAP
INSTRUCT. REG
OPTIONAL REG
BP
Gen
Ana
Gen
Ana
Ana
Gen
Ana
Thank you.....